T. HOEFLER, M. PUESCHEL

Lecture 9: Finishing consensus, scalable lock study, and oblivious algorithms

Teaching assistant: Salvatore Di Girolamo

Motivational video: https://www.youtube.com/watch?v=qx2dRIQXnbs
The simplest networking question: ping pong latency!

The latency of Piz Dora is 1.77us!
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The latency of Piz Dora is 1.77us!

How did you get to this?
The latency of Piz Dora is 1.77us!

I averaged $10^6$ tests, it must be right!

How did you get to this?
The simplest networking question: ping pong latency!

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I averaged $10^6$ tests, it must be right!

How did you get to this?

Why do you think so? Can I see the data?
The simplest networking question: ping pong latency!

The latency of Piz Dora is 1.77us!

How did you get to this?

I averaged $10^6$ tests, it must be right!

Why do you think so? Can I see the data?
The simplest networking question: ping pong latency!

The latency of Piz Dora is 1.77μs! How did you get to this? I averaged 10^6 tests, it must be right!

Why do you think so? Can I see the data?

The simplest networking question: ping pong latency!

Rule 5: Report if the measurement values are deterministic. For nondeterministic data, report confidence intervals of the measurement.

- CIs allow us to compute the number of required measurements!
- Can be very simple, e.g., single sentence in evaluation: “We collected measurements until the 99% confidence interval was within 5% of our reported means.”
Thou shalt not trust your average textbook!

The confidence interval is 1.765us to 1.775us
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The confidence interval is 1.765us to 1.775us

Did you assume normality?
Thou shalt not trust your average textbook!

The confidence interval is 1.765us to 1.775us

Did you assume normality?

Yes, I used the central limit theorem to normalize by summing subsets of size 100!
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The confidence interval is 1.765us to 1.775us

Yes, I used the central limit theorem to normalize by summing subsets of size 100!

Can we test for normality?

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The confidence interval is 1.765us to 1.775us

Ugs, the data is not normal at all! The real CI is actually 1.6us to 1.9us!

Can we test for normality?

Thou shalt not trust your average textbook!

Rule 6: Do not assume normality of collected data (e.g., based on the number of samples) without diagnostic checking.

- Most events will slow down performance
  - Heavy right-tailed distributions

- The Central Limit Theorem only applies asymptotically
  - Some papers/textbook mention “30-40 samples”, don’t trust them!
Thou shalt not trust your system!

Look what data I got!

Clearly, the mean/median are not sufficient!

Try quantile regression!
Thou shalt not trust your system!

Look what data I got!

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Image credit: nersc.gov

<table>
<thead>
<tr>
<th>Piz Dora</th>
<th>Min: 1.57</th>
<th>Max: 7.2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Median</td>
<td>Arithmetic Mean</td>
</tr>
<tr>
<td></td>
<td>99% CI (Mean)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pilatus</th>
<th>Min: 1.48</th>
<th>Max: 11.59</th>
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Wow, so Pilatus is better for (worst-case) latency-critical workloads even though Dora is expected to be faster.
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Rule 8: Carefully investigate if measures of central tendency such as mean or median are useful to report. Some problems, such as worst-case latency, may require other percentiles.

Final project presentation: last Monday 12/17 during lecture
  - Report will be due in January!
    Starting to write early is very helpful --- write – rewrite – rewrite (no joke!)
  - Coordinate your talk! You have 10 minutes (8 talk + 2 Q&A)
    What happened since the intermediate report?
    Focus on the key aspects (time is tight)!
    Try to wrap up – only minor things left for final report.
    Engage the audience 😊

Send slides by Sunday night (11:59pm Zurich time) to Salvatore!
  - We will use a single (windows) laptop to avoid delays when switching
  - Expect only Windows (powerpoint) or a PDF viewer
  - The order of talks will again be randomized for fairness
Review of last lecture(s)

- **Lock implementation(s)**
  - Advanced locks (CLH + MCS)

- **Started impossibility of wait-free consensus with atomic registers**
  - “perhaps one of the most striking impossibility results in Computer Science” (Herlihy, Shavit)
    
    *Will continue/finish proof today as starter!*

- **Theoretical background for performance**
  - Amdahl’s law
  - Models: PRAM, Work/Depth, simple alpha-beta (Hockney) model
  - Simple algorithms: reduce, scan, mergesort,
  - Brent’s scheduling lemma + Little’s law
  - Greedy scheduling + random work stealing

- **Practical performance**
  - Roofline and balance modeling for practical performance optimization
  - Vectorization
Learning goals for today

- Quickly recap consensus and first part of valence proof
  - impossibility of atomic registers for wait-free consensus
  - Complete proof together

- Case study about scalable locking
  - Complete correctness section!

- Oblivious algorithms
  - How do work-depth graphs relate to practice?

- Strict optimality
  - Work/depth tradeoffs and bounds

- Applications of prefix sums
  - Parallelize seemingly sequential algorithms
DPHPC Overview

DPHPC

- locality
  - caches
  - memory hierarchy
- parallelism
  - vector ISA
  - shared memory
  - distributed memory

- cache coherency

- memory models
  - locks
    - lock free
    - wait free
    - linearizability
- distributed algorithms
- group communications

- Amdahl's and Gustafson's law

- models
  - memory 
    - $\alpha - \beta$
  - PRAM
  - LogP

- I/O complexity balance principles I
- Little's Law balance principles II
- scheduling
Remember: lock-free vs. wait-free

- A locked method
- A lock-free method
- A wait-free method
Remember: lock-free vs. wait-free

- A locked method
  - May deadlock (methods may never finish)

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  - Guarantees that infinitely often some method call finishes in a finite number of steps

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- A wait-free method
  - Guarantees that **each** method call finishes in a finite number of steps (implies lock-free)
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- **Synchronization instructions are not equally powerful!**
  - Indeed, they form an infinite hierarchy; no instruction (primitive) in level x can be used for lock-/wait-free implementations of primitives in level z>x.
Concept: Consensus Number

- Each level of the hierarchy has a “consensus number” assigned.
  - Is the maximum number of threads for which primitives in level x can solve the consensus problem

- The consensus problem:
  - Has single function: decide(v)
  - Each thread calls it at most once, the function returns a value that meets two conditions:
    - **consistency**: all threads get the same value
    - **validity**: the value is some thread’s input
  - Simplification: binary consensus (inputs in {0,1})
Understanding Consensus

- Can a particular class solve n-thread consensus wait-free?
  - A class C solves n-thread consensus if there exists a consensus protocol using any number of objects of class C and any number of atomic registers
  - The protocol has to be wait-free (bounded number of steps per thread)
  - The consensus number of a class C is the largest n for which that class solves n-thread consensus (may be infinite)
  - Assume we have a class D whose objects can be constructed from objects out of class C. If class C has consensus number n, what does class D have?
Starting simple ...

- Binary consensus with two threads (A, B):
  - Each thread moves until it decides on a value
  - May update shared objects
  - Protocol state = state of threads + state of shared objects
  - Initial state = state before any thread moved
  - Final state = state after all threads finished
  - States form a tree, wait-free property guarantees a finite tree
    
    Example with two threads and two moves each!

- Define various states
  - Bivalent, univalent, critical

- Two helper lemmata
  - Lemma 1: the initial state is bivalent
  - Lemma 2: every wait-free consensus protocol has a critical state
Atomic Registers

- Theorem [Herlihy’91]: Atomic registers have consensus number one
  - I.e., they cannot be used to solve even two-thread consensus! Really?
Atomic Registers

- **Theorem [Herlihy’91]:** Atomic registers have consensus number one
  - I.e., they cannot be used to solve even two-thread consensus! Really?
- **Proof outline:**
  - Assume arbitrary consensus protocol, thread A, B
  - Run until it reaches critical state where next action determines outcome (show that it must have a critical state first)
  - Show all options using atomic registers and show that they cannot be used to determine one outcome for all possible executions!
  1. Any thread reads (other thread runs solo until end)
  2. Threads write to different registers (order doesn’t matter)
  3. Threads write to same register (solo thread can start after each write)
Atomic Registers

- Theorem [Herlihy’91]: Atomic registers have consensus number one
- Corollary: It is impossible to construct a wait-free implementation of any object with consensus number of >1 using atomic registers
  - “perhaps one of the most striking impossibility results in Computer Science” (Herlihy, Shavit)
  - \( \rightarrow \) We need hardware atomics or Transactional Memory!
- Proof technique borrowed from:

  Impossibility of distributed consensus with one ... - ACM Digital Library
  https://dl.acm.org/citation.cfm?id=214121
  by MJ Fischer - 1985 - Cited by 4669 - Related articles
  Sep 4, 2012 - Michael J. Fischer, Nancy A. Lynch, Michael S. Paterson, Impossibility of distributed consensus with one faulty process, Proceedings of the ...

- Very influential paper, always worth a read!
  - Nicely shows proof techniques that are central to parallel and distributed computing!
Other Atomic Operations

- Simple RMW operations (Test&Set, Fetch&Op, Swap, basically all functions where the op commutes or overwrites) have consensus number 2!
  - Similar proof technique (bivalence argument)
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- CAS and TM have consensus number $\infty$
  - Constructive proof:

```c
const int first = -1
volatile int thread = -1;
int proposed[n];

int decide(v) {
    proposed[tid] = v;
    if(CAS(thread, first, tid))
        return v; // I won!
    else
        return proposed[thread]; // thread won
}
```
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- Machines providing CAS are asynchronous computation equivalents of the Turing Machine
  i.e., any concurrent object can be implemented in a wait-free manner (not necessarily fast!)
Now you know everything about parallel program correctness 😊

- At least a lot ... ;-)  
  - We’ll argue more about *performance* now!

- You have all the tools for:
  - Efficient locks
  - Efficient lock-based algorithms
  - Reasoning about parallelism!

- What now?
  - Now you understand practice and will appreciate theory
    - *Wasn’t that all too messy 😊?*
  - Focus on (parallel) performance, techniques, and algorithms

- But let’s start with another case study about locks
  - Research (best) paper published at a top-tier conference some years ago
    - *So you get a feeling of the field – and deepen understanding of MCS locks in practice*
Case study: Fast Large-scale Locking in Practice
Case study: Fast Large-scale Locking in Practice
Case study: Fast Large-scale Locking in Practice
Case study: Fast Large-scale Locking in Practice

structure

Proc p

lock

Proc q
Case study: Fast Large-scale Locking in Practice
Case study: Fast Large-scale Locking in Practice

structure

Proc p

lock

accesses

unlock

Proc q
Case study: Fast Large-scale Locking in Practice
Case study: Fast Large-scale Locking in Practice

Inuitive semantics

structure

Proc p

lock

accesses

unlock

Proc q

lock

accesses
Case study: Fast Large-scale Locking in Practice

Inuitive semantics

Various performance penalties

lock
accesses
unlock

lock
accesses
Locks: Challenges
Locks: Challenges
Locks: Challenges
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Locks: Challenges
Locks: Challenges

Calciu et al.: NUMA-aware reader-writer locks, PPoPP’13
Locks: Challenges
Locks: Challenges
Locks: Challenges

We need intra- and inter-node topology-awareness

We need to cover arbitrary topologies
Locks: Challenges
Locks: Challenges
Locks: Challenges

Locks: Challenges

Locks: Challenges

Locks: Challenges

We need to distinguish between readers and writers

We need to distinguish between readers and writers

We need flexible performance for both types of processes

What will we use in the design?
Ingredient 1 - MCS Locks

- Proc cannot enter
- Next proc
- Pointer to the queue tail

Procedure (Proc) cannot enter the next procedure (Next proc) until the queue tail is accessed and updated.

Mellor-Crummey and Scott: Algorithms for Scalable Synchronization on Shared-Memory Multiprocessors, ACM TOCS'91
Ingredient 1 - MCS Locks

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Ingredient 2 - Reader-Writer Locks
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How to manage the design complexity?
How to manage the design complexity?

What mechanism to use for efficient implementation?
How to manage the design complexity?

How to ensure tunable performance?

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What mechanism to use for efficient implementation?
REMOTE MEMORY ACCESS (RMA) PROGRAMMING
REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory

A
REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory

A

Process q

Memory

B

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory
A

Process q

Memory
B

Cray
BlueWaters

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p
Memory A

Process q
Memory B

Cray BlueWaters

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory

A

Cray BlueWaters

Process q

Memory

B

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p
Memory
A

Process q
Memory
B

Cray
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REMOTE MEMORY ACCESS (RMA) PROGRAMMING

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory

A

B

Process q

Memory

A

B

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

Process p

Memory

A

B

Process q

Memory

A

B

A put

get B

flush

Cray

BlueWaters

REMOTE MEMORY ACCESS (RMA) PROGRAMMING

REMOTE MEMORY ACCESS PROGRAMMING

- Implemented in hardware in NICs in the majority of HPC networks (RDMA support).
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RMA-RW - Required Operations

Process p

Memory

Process q

Memory

3
3
3
3
RMA-RW - Required Operations

Process p

Memory

6 put

Process q

Memory

3

3

3

3

3
RMA-RW - Required Operations

Process p
Memory

6 put

Process q
Memory
6
3
3
3
3
RMA-RW - Required Operations

Process p

Memory

Process q

Memory

6 put

get

6

3

3

3
RMA-RW - Required Operations

Process p

Memory

3

Process q

Memory

3

3

3

3

3

3

3

6 put

get

6
RMA-RW - Required Operations

Process p

Memory

3

6 put

get

6 Fetch-and-Add (FAA)

3

Process q

Memory

3

6

3

3

3

3
RMA-RW - Required Operations

Process p

- Memory

3

Process q

- Memory

3

3

3

6 put

get

6 Fetch-and-Add (FAA)

6
RMA-RW - Required Operations

- Process p
  - Memory
  - 6 put
  - 3 get
  - 3 Fetch-and-Add (FAA)

- Process q
  - Memory
  - 6
  - 3
  - 9
  - 3
  - 3
RMA-RW - Required Operations

Required Operations

- Put
- Get
- Fetch-and-Add (FAA)
- Replace
RMA-RW - Required Operations

Process p
- Memory
  - 3
  - 6 put
  - 3
  - 6 Fetch-and-Add (FAA)
  - 3
  - 6 replace

Process q
- Memory
  - 6
  - 3
  - 6 get
  - 3
  - 9
  - 6 replace
  - 3
RMA-RW - Required Operations

**Process p**

- **Memory**
  - **put** (6)
  - **get**
  - **Fetch-and-Add (FAA)** (6)
  - **replace** (6)
  - **Compare-and-Swap (CAS)** (8)

**Process q**

- **Memory**
  - **put** (6)
  - **get** (3)
  - **Fetch-and-Add (FAA)** (6)
  - **replace** (6)
  - **Compare-and-Swap (CAS)** (3)
RMA-RW - Required Operations

Process p

Memory

- 6 put
- 3
- 6 Fetch-and-Add (FAA)
- 3
- 6 replace
- 3
- 3
- 8 Compare-and-Swap (CAS)
- 3

Process q

Memory

- 6
- 3
- 6
- 9

Required Operations
RMA-RW - Required Operations

Process p

Memory

Process q

Memory

- **put**: 6
- **get**: 3 (from Process p) → 6 (to Process q)
- **Fetch-and-Add (FAA)**: 6 (from Process p) → 9 (to Process q)
- **replace**: 3 (from Process p) → 6 (to Process q)
- **Compare-and-Swap (CAS)**: 3 (from Process p) → 3 (to Process q)
MPI RMA primer ([much] more in the recitation sessions)

- **Windows expose memory**
  - Created explicitly

- **Remote accesses**
  - Put, get
  - Atomics
    - Accumulate (also atomic Put)
    - Get_accumulate (also atomic Get)
    - Fetch and op (faster single-word get_accumulate)
    - Compare and swap

- **Synchronization**
  - Two modes: passive and active target
    - We use passive target today, similar to shared memory!
    - Synchronization: flush, flush_local

- **Memory model**
  - Unified (coherent) and separate (not coherent) view - it’s complicated but versatile
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Modular design

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Modular design

R2 R1
W1

R3 R4
W2 W3

R5 R6 R7
W4 W5

R8 R9
W6 W7 W8

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Each element has its own distributed MCS queue (DQ) of writers

Modular design

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How to manage the design complexity?

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P. Schmid, M. Besta, TH: High-Performance Distributed RMA Locks, ACM HPDC’16, best paper
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Modular design.
How to ensure tunable performance?
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A tradeoff parameter for every structure

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Each DQ: fairness vs throughput of writers

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DT: a parameter for the throughput of readers vs writers

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DC: a parameter for the latency of readers vs writers

DT: a parameter for the throughput of readers vs writers

A tradeoff parameter for every structure
Distributed MCS Queues (DQs) - Throughput vs Fairness

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Each DQ: The maximum number of lock passings within a DQ at level i, before it is passed to another \( T_{L,i} \) DQ at i.

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Distributed MCS Queues (DQs) - Throughput vs Fairness

Each DQ: The maximum number of lock passings within a DQ at level i, before it is passed to another DLQ at i.

Larger $T_{L,i}$: more throughput at level i. Smaller $T_{L,i}$: more fairness at level i.

- $T_{L,1}$
- $T_{L,2}$
- $T_{L,3}$

W1, W2, W3, W4, W5, W6, W7, W8

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Distributed Tree of Queues (DT) - Throughput of readers vs writers

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Distributed Tree of Queues (DT) - Throughput of readers vs writers

DT: The maximum number of consecutive lock passings within readers ($T_R$).

$T_{L,1}$

$T_{L,2}$

$T_{L,3}$

W1 $\rightarrow$ W2 $\rightarrow$ W3 $\rightarrow$ W4 $\rightarrow$ W5 $\rightarrow$ W6 $\rightarrow$ W7 $\rightarrow$ W8

W3 $\rightarrow$ W8

W5 $\rightarrow$ W8

W1 $\rightarrow$ W3

W1 $\rightarrow$ W3

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Distributed Counter (DC) - Latency of readers vs writers
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DC: every $k$th compute node hosts a partial counter, all of which constitute the DC.

$k = T_{DC}$
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A writer holds the lock $b|x|y$

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$T_{DC} = 1$

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DC: every $k$th compute node hosts a partial counter, all of which constitute the DC.

$$k = T_{DC}$$

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Readers that arrived at the CS

Readers that left the CS

$$T_{DC} = 2$$
Distributed Counter (DC) - Latency of readers vs writers

DC: every $k$th compute node hosts a partial counter, all of which constitute the DC.

$$k = T_{DC}$$

A writer holds the lock $b|x|y$

Readers that arrived at the CS

Readers that left the CS

$$T_{DC} = 2$$
Design space
Design space

P. Schmid, M. Besta, TH: High-Performance Distributed RMA Locks, ACM HPDC’16, best paper
Design space

\[ T_R \]
Design space

Higher throughput of *writers* vs *readers*

\[ T_R \]

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Design space

Higher throughput of **writers** vs **readers**

$T_D$  
$T_R$  

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Higher throughput of writers vs readers

Lower latency of writers vs readers

Design space

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Design space

Lower latency of writers vs readers

Higher throughput of writers vs readers

\( T_{DC} \)

\( T_{L,i} \)

\( T_R \)
Design space

Higher throughput of **writers** vs **readers**

Locality vs fairness (for writers)

Lower latency of **writers** vs **readers**

P. Schmid, M. Besta, TH: High-Performance Distributed RMA LOCKs, ACM HPDC’16, best paper
Design space

Higher throughput of writers vs readers

Locality vs fairness (for writers)

Lower latency of writers vs readers

\( T_{DC} \)

\( T_{L,i} \)

\( T_R \)
Design space

- **Higher throughput of writers vs readers**
- **Locality vs fairness (for writers)**

**Designs:**
- **Design A**
- **Design B**
Lock Acquire by Readers

A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation

P. Schmid, M. Besta, TH: High-Performance Distributed RMA Locks, ACM HPDC'16, best paper
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A writer holds the lock
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Readers that left the CS

0|7|7
R1
R2

0|1|1
R4
R3

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Lock Acquire by Readers

A lightweight acquire protocol for readers: only one atomic fetch-and-add (FAA) operation

0|8|7
R1
FAA
R2

0|3|1
R4
FAA
R3

A writer holds the lock

Readers that arrived at the CS

b|x|y

Readers that left the CS

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Acquire MCS

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Lock Acquire by Writers

Acquire MCS

0|9|9

0|3|3

0|8|8

0|5|5

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Lock Acquire by Writers

Acquire the main MCS lock

Acquire MCS

Acquire MCS

W9 → W3 → W8

W9 → W1 → W3

W5 → W8

W4 → W5

W6 → W7 → W8

0|3|3

0|8|8

0|5|5

W9 → W1

W2 → W3

W9 → W1

W1

W4

W5

W6

W7

W8

Acquire the main MCS lock

Acquire MCS

Acquire MCS

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Acquire the main MCS lock

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Acquire the main MCS lock

Acquire MCS

Acquire MCS

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Lock Acquire by Writers

Acquire the main MCS lock

W8

Acquire MCS

W9 W3 W8

Acquire MCS

W9 W1 W3

W9 W1

W5 W8

W5 W8

W6 W7 W8
Acquire the main MCS lock.
Lock Acquire by Writers

Acquire the main lock

Acquire MCS

W9 → W1 → W3

Acquire MCS

W9 → W2 → W3

Acquire MCS

W9 → W4 → W5

Acquire the main MCS lock

W9 → W5 → W8
EVALUATION

- CSCS Piz Daint (Cray XC30)
- 5272 compute nodes
- 8 cores per node
- 169TB memory

- Microbenchmarks: acquire/release: latency, throughput
- Distributed hashtable
Evaluation - Distributed Counter Analysis

Throughput, 2% writers
Single-operation benchmark

P. Schmid, M. Besta, TH: High-Performance Distributed RMA Locks, ACM HPDC’16, best paper
Evaluation - Reader Threshold Analysis

Throughput, 0.2% writers,
Empty-critical-section benchmark

Throughput [mln locks/s]

MPI processes (P)

P. Schmid, M. Besta, TH: High-Performance Distributed RMA Locks, ACM HPDC’16, best paper
Evaluation - Comparison to the State-of-the-Art

Evaluation - Comparison to the State-of-the-Art

Throughput, single-operation benchmark

Evaluation - Distributed Hashtable

20% writers

10% writers

Evaluation - Distributed Hashtable

2% of writers

0% of writers

Another application area - Databases

- MPI-RMA for distributed databases?

Hash-Join

Sort-Join

C. Barthels, et al., TH: Distributed Join Algorithms on Thousands of Cores presented in Munich, Germany, VLDB Endowment, Aug. 2017
Another application area - Databases

- MPI-RMA for distributed databases on Piz Daint

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Another application area - Databases

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Now on to parallel algorithms!

- **Oblivious parallel algorithms**
  - Fixed structure work-depth graphs

- **Nonoblivious parallel algorithms**
  - Data-dependent structure work-depth graphs

- **Data movement and I/O complexity**
  - Communication complexity
Work/Depth in Practice – Oblivious Algorithms

“An algorithm is execution-oblivious if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs”
Work/Depth in Practice – Oblivious Algorithms

“An algorithm is **execution-oblative** if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs”

Execution oblivious or not?
Work/Depth in Practice – Oblivious Algorithms

“An algorithm is execution-oblivious if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs”

Execution oblivious or not?

```c
int reduce(int n, arr[n]) {
    for(int i=0; i<n; ++i)
        sum += arr[i];
}
```
"An algorithm is execution-oblivious if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs"
An algorithm is **execution-oblivious** if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs.

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int findmin(int n, a[n]) {
    for(int i=1; i<n; i++)
        if(a[i]<a[0]) a[0] = a[i];
}

int finditem(list_t list) {
    item = list.head;
    while(item.value!=0 && item.next!=NULL)
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Execution oblivious or not?

- Quicksort?

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**Execution oblivious or not?**

- Quicksort?
- Prefix sum on an array?

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- Simple dense matrix multiplication?

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- Quicksort?
- Prefix sum on an array?
- Simple dense matrix multiplication?
- Dense matrix vector product?

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- Dense matrix vector product?
- Sparse matrix vector product?

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Execution oblivious or not?

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- Prefix sum on an array?
- Simple dense matrix multiplication?
- Dense matrix vector product?
- Sparse matrix vector product?
- Queue-based breadth-first search?

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Obliviousness as property of an execution

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```

- Class question: Can an algorithm decide whether a program is oblivious or not?
Obliviousness as property of an execution

“An algorithm is execution-oblivious if, for each problem size, the sequence of instructions executed, the set of memory locations read and the set of memory locations written by each executed instruction are determined by the input size and are independent of the values of the other inputs”

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Structural obliviousness as stronger property

“A program is **structurally-oblivious** if any value used in a conditional branch, and any value used to compute indices or pointers is structurally-dependent only in the input variable(s) that contains the problem size but not on any other input”
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Structurally oblivious or not?

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int reduce(int n, arr[n]) {
    for(int i=0; i<n; ++i)
        sum += arr[i];
}
```
Structural obliviousness as stronger property

“A program is **structurally-oblivious** if any value used in a conditional branch, and any value used to compute indices or pointers is structurally-dependent only in the input variable(s) that contains the problem size but not on any other input”

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int oblivious(int n, a[n], b[n]) {
    for(int i=0; i<n; ++i) {
        x = a[i] + 1;
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```c
int finditem(list_t list) {
    item = list.head;
    while(item.value!=0 && item.next!=NULL) {
        item = item.next;
    }
}
```
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- **Clear that structurally oblivious programs are also execution oblivious**
  - Can be programmatically (statically decided)
  - Sufficient for practical use
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### Structurally oblivious or not?

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- **Clear that structurally oblivious programs are also execution oblivious**
  - Can be programmatically (statically decided)
  - Sufficient for practical use

- **The middle example is not structurally oblivious but execution oblivious**
  - First branch is always taken (assuming no overflow) but static dependency analysis is conservative
Why obliviousness?

We can easily reason about oblivious algorithms

- Execution DAG can be constructed “statically”
- We have done this in the last weeks intuitively but you never asked how to do it for BFS for example 😊

\[ \log_2 n \]

Are both W and D optimal?

Yes!
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- Simple example (that you know): parallel summation

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  - Question: what is \( W(n) \) and \( D(n) \) of sequential summation?

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  *Separate for \( W \) and \( D \)! Typically try to achieve both!*

\[ \log_2 n \]

Are both \( W \) and \( D \) optimal?

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    ▪ Question: what is $W(n)$ and $D(n)$ of the optimal parallel summation?
      $$\log_2 n \lceil$$
      *Are both $W$ and $D$ optimal?*
      *Yes!*
Why obliviousness?

\[
\log_2 n \left\lceil \log_2 \log_2 n \right\rceil \log_2 n
\]

We can easily reason about oblivious algorithms

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    \[ W(n) = D(n) = n - 1 \]
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    *Separate for W and D! Typically try to achieve both!*
  - Question: what is W(n) and D(n) of the optimal parallel summation?
    \[ W(n) = n - 1 \quad D(n) = \lceil \log_2 n \rceil \]
    Are both W and D optimal?  
    Yes!
Why obliviousness?

\[ \log_2 n \] \log_2 2 \log_2 2 \log_2 n \log_2 n \]

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    Are both W and D optimal?
    Yes!
Why obliviousness?

\[
\log 2 \ n \mid \log 2 \log 2 \ 2 \log 2 \ n \mid nn \mid \log 2 \ n
\]

We can easily reason about oblivious algorithms

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- Simple example (that you know): parallel summation
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    \[
    W(n)=D(n)=n-1
    \]
  - Question: is this optimal? How would you define optimality?
    
    Separate for W and D! Typically try to achieve both!

  - Question: what is W(n) and D(n) of the optimal parallel summation?
    
    Are both W and D optimal?
    
    Yes!
    
    Yes!
Starting simple: optimality?

- Next example you know: scan!
  - For a vector \([x_1, x_2, \ldots, x_n]\) compute vector of n results: \([x_1; x_1 + x_2; x_1 + x_2 + x_3; \ldots; x_1 + x_2 + x_i \ldots + x_{n-1} + x_n]\)
  - Simple serial schedule
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\[x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5 \quad x_6 \quad x_7 \quad x_8\]
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- **Next example you know: scan!**
  - For a vector \([x_1, x_2, \ldots, x_n]\) compute vector of \(n\) results: \([x_1; x_1 \cdot x_2; x_1 \cdot x_2 \cdot x_3; \ldots; x_1 + x_2 + x_i \ldots + x_{n-1} + x_n]\)
  - Simple serial schedule

```
x_1 -> x_2 -> x_3 -> x_4 -> x_5 -> x_6 -> x_7 -> x_8
```

```
\sum
```

```
x_1 -> x_1 + x_2
```
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\[
\begin{align*}
&x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \\
&\downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
&x_1 & x_1 + x_2 & \sum & \sum & \sum & \sum & \sum & \sum \\
&\downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
&x_1 & x_1 + x_2
\end{align*}
\]
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  - Simple serial schedule

```
\begin{align*}
  x_1 &\rightarrow & x_1 + x_2 &\rightarrow & x_1 + x_2 + x_3 &\rightarrow & \ldots &\rightarrow & x_1 + x_2 + x_3 + \ldots + x_4 \\
  x_1 + x_2 &\rightarrow & x_1 + x_2 + x_3 & \rightarrow & \ldots &\rightarrow & x_1 + x_2 + x_3 + \ldots + x_4 \rightarrow & \ldots &\rightarrow & x_1 + \ldots + x_5 \\
  x_1 + x_2 + x_3 &\rightarrow & \ldots &\rightarrow & x_1 + \ldots + x_n \\
\end{align*}
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![Diagram of vector operations](image)
Starting simple: optimality?

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  - Simple serial schedule

![Diagram showing a simple serial schedule for computing a vector of results from a given vector.](image-url)
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  - For a vector \([x_1, x_2, ..., x_n]\) compute vector of \(n\) results: \([x_1; x_1 + x_2; x_1 + x_2 + x_3; ...; x_1 + x_2 + x_i ... + x_{n-1} + x_n]\)
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Class question: work and depth?
Starting simple: optimality?

- Next example you know: scan!
  - For a vector \([x_1, x_2, \ldots, x_n]\) compute vector of n results: \([x_1; x_1 + x_2; x_1 + x_2 + x_3; \ldots; x_1 + x_2 + x_i \ldots + x_{n-1} + x_n]\)
  - Simple serial schedule

```
\begin{center}
\begin{tikzpicture}[node distance=2cm]
    \node (x1) {$x_1$};
    \node (x2) [right of=x1] {$x_2$};
    \node (x3) [right of=x2] {$x_3$};
    \node (x4) [right of=x3] {$x_4$};
    \node (x5) [right of=x4] {$x_5$};
    \node (x6) [right of=x5] {$x_6$};
    \node (x7) [right of=x6] {$x_7$};
    \node (x8) [right of=x7] {$x_8$};

    \draw[->] (x1) -- node[below] {$x_1$} (x2);
    \draw[->] (x2) -- node[below] {$x_1 + x_2$} (x3);
    \draw[->] (x3) -- node[below] {$x_1 + \ldots + x_3$} (x4);
    \draw[->] (x4) -- node[below] {$x_1 + \ldots + x_4$} (x5);
    \draw[->] (x5) -- node[below] {$x_1 + \ldots + x_5$} (x6);
    \draw[->] (x6) -- node[below] {$x_1 + \ldots + x_6$} (x7);
    \draw[->] (x7) -- node[below] {$x_1 + \ldots + x_7$} (x8);
    \draw[->] (x8) -- node[below] {$x_1 + \ldots + x_8$} (x1);

    \draw[->] (x1) -- node[above] {$\sum$} (x2);
    \draw[->] (x2) -- node[above] {$\sum$} (x3);
    \draw[->] (x3) -- node[above] {$\sum$} (x4);
    \draw[->] (x4) -- node[above] {$\sum$} (x5);
    \draw[->] (x5) -- node[above] {$\sum$} (x6);
    \draw[->] (x6) -- node[above] {$\sum$} (x7);
    \draw[->] (x7) -- node[above] {$\sum$} (x8);
\end{tikzpicture}
\end{center}
```

Class question: work and depth?

\[ W(n) = n-1, \quad D(n) = n-1 \]
Starting simple: optimality?

- Next example you know: scan!
  - For a vector \([x_1, x_2, ..., x_n]\) compute vector of n results: \([x_1; x_1 + x_2; x_1 + x_2 + x_3; ...; x_1 + x_2 + x_i ... + x_{n-1} + x_n]\)
  - Simple serial schedule

Class question: work and depth?

\[W(n) = n-1, \; D(n) = n-1\]

Class question: is this optimal?
What did we learn earlier?

- Recursive to get to $W = O(n)$ and $D = O(\log n)$! Assume $n = 2^k$ for simplicity!
  - Sounds “optimal”, doesn’t it? Well, let’s look at the constants!
- Algorithm
What did we learn earlier?

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![Diagram](image)
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Class question: work?
(hint: after the way up, all powers of two are done, all others require another operation each)
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(hint: after the way up, all powers of two are done, all others require another operation each)

$$W(n) = 2n - \log_2 n - 1$$
What did we learn earlier?

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\[
W(n) = 2n - \log_2 n - 1
\]

Class question: depth?
(needs to go up and down the tree)
What did we learn earlier?

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Class question: work?
(hint: after the way up, all powers of two are done, all others require another operation each)

$$W(n) = 2n - \log_2 n - 1$$

Class question: depth?
(needs to go up and down the tree)

$$D(n) = 2 \log_2 n - 1$$
What did we learn earlier?

- Recursive to get to $W = O(n)$ and $D = O(\log n)$! Assume $n = 2^k$ for simplicity!
  - Sounds “optimal”, doesn’t it? Well, let’s look at the constants!
- Algorithm

```
\[
\begin{align*}
W(n) &= 2n - \log_2 n - 1 \\
D(n) &= 2 \log_2 n - 1
\end{align*}
\]
```

Class question: what happened to optimality?
Oh no, not good, another algorithm to the rescue!

- Dissemination/recursive doubling – another well-known algorithmic technique – similar to trees
Oh no, not good, another algorithm to the rescue!

- Dissemination/recursive doubling – another well-known algorithmic technique – similar to trees

\[ x_1 \quad x_2 \quad x_3 \quad x_4 \quad x_5 \quad x_6 \quad x_7 \quad x_8 \]
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(hint: number of count number of omitted ops)
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Class question: work?
(hint: number of count number of omitted ops)

\[ W(n) = n \log_2 n - n + 1 \]
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(hint: number of count number of omitted ops)

\[ W(n) = n \log_2 n - n + 1 \]

Class question: depth?

\[ D(n) = 2 \log_2 n \]

Class question: is this now optimal?
Oh no, three non-optimal algorithms so far!

- **Obvious question: is there a depth- and work-optimal algorithm?**
  - This took years to settle! The answer is surprisingly: no
  - We know, for parallel prefix: $W + D \geq 2n - 2$
Oh no, three non-optimal algorithms so far!

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\[ x_1 \ x_2 \ x_3 \ x_4 \ x_5 \ x_6 \ x_7 \ x_8 \]
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Output tree:
- leaves are all inputs, rooted at \( x_n \)
- binary due to binary operation
- \( W = n - 1, D = D_o \)
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Oh no, three non-optimal algorithms so far!

- **Obvious question: is there a depth- and work-optimal algorithm?**
  - This took years to settle! The answer is surprisingly: no
  - We know, for parallel prefix: \( W + D \geq 2n - 2 \)

Output tree:
- leaves are all inputs, rooted at \( x_n \)
- binary due to binary operation
- \( W = n - 1, D = D_o \)

Input tree:
- rooted at \( x_1 \), leaves are all outputs
- not binary (simultaneous read)
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Input tree:
- rooted at $x_1$, leaves are all outputs
- not binary (simultaneous read)
- $W = n - 1$

Ridge can be at most $D_o$ long!
Now add trees and subtract shared vertices:
$(n - 1) + (n - 1) - D_o = 2n - 2 - D_o \leq W$

q.e.d.
Work-Depth Tradeoffs and deficiency

“The deficiency of a prefix circuit $c$ is defined as $\text{def}(c) = W_c + D_c - (2n - 2)$”

Latest 2006 result for zero-deficiency construction for $n > F(D + 3) - 1$ ($f(n)$ is inverse)

From Zhu et al.: “Construction of Zero-Deficiency Parallel Prefix Circuits”
Work- and depth-optimal constructions

Work-optimal?

- $= n - 1$, thus $D = 2n - 2 - W = n - 1$ q.e.d. ☺

Depth-optimal?

- Ladner and Fischer propose a construction for work-efficient circuits with minimal depth $D = \lceil \log_2 n \rceil$, $W \leq 4n$

  Simple set of recursive construction rules (boring for class, check 1980’s paper if needed)

  Has an unbounded fan-out! May thus not be practical ☹

Depth-optimal with bounded fan-out?

- Some constructions exist, interesting open problem
- Nice research topic to define optimal circuits
Work- and depth-optimal constructions

Work-optimal?
- Only sequential! Why?
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**Work- and depth-optimal constructions**

\[ n - 1, \text{ thus } D = 2n - 2 - W = n - 1 \quad \text{q.e.d.} \]

Work-optimal?
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- Ladner and Fischer propose a construction for work-efficient circuits with minimal depth
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Work- and depth-optimal constructions

\[ nn-1, \text{ thus } DD=2nn-2-WW=nn-1 \quad \text{q.e.d.} \]

Work-optimal?
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- \[ W = n - 1, \text{ thus } D = 2n - 2 - W = n - 1 \quad \text{q.e.d.} \]

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Work- and depth-optimal constructions

\[
\left\lceil \log_2 n \right\rceil \log_2 \log_2 2 2 \log_2 n \right\rceil nn/ \log_2 n/, WW \leq 4nn
\]

\(nn-1\), thus \(DD=2nn-2-WW=nn-1\) q.e.d. ️

Work-optimal?
- Only sequential! Why?
- \(W = n - 1\), thus \(D = 2n - 2 - W = n - 1\) q.e.d. ⚡️

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Work- and depth-optimal constructions

$\lceil \log_2 n \rceil \log_2 \log_2 2 2 \log_2 n \rceil$ $\leq 4n$, $WW \leq 4nn$

$n - 1$, thus $DD = 2nn - 2 - WW = nn - 1$ q.e.d.

Work-optimal?
- Only sequential! Why?
- $W = n - 1$, thus $D = 2n - 2 - W = n - 1$ q.e.d.

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Depth-optimal with bounded fan-out?

Depth-optimal with bounded fan-out?
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Work- and depth-optimal constructions

\[ \lceil \log_2 n \rceil \log_2 \log_2 2^2 \log_2 2 \log_2 n \rceil \quad nW \leq 4nn \]

\( nn-1, \text{ thus } DD=2nn-2-WW=nn-1 \text{ q.e.d. } \)

Work-optimal?
- Only sequential! Why?
- \( W = n-1, \text{ thus } D = 2n-2-W = n-1 \text{ q.e.d. } \)

Depth-optimal?
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Work- and depth-optimal constructions

\[ \lceil \log_2 n \rceil \log_2 \log_2 2 \log_2 2 \log_2 n \rceil \log_2 n \rceil, WW \leq 4nn \]

\( nn-1, \text{thus} D = 2nn - 2 - WW = nn - 1 \text{ q.e.d.} \)

Work-optimal?
- Only sequential! Why?
- \( W = n - 1, \text{thus} D = 2n - 2 - W = n - 1 \text{ q.e.d.} \)

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Depth-optimal with bounded fan-out?
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- Nice research topic to define optimal circuits
But why do we care about this prefix sum so much?

It’s the simplest problem to demonstrate W-D tradeoffs
- And it’s one of the most important parallel primitives

\[ a + b \text{ (n-bit numbers)} \]
- Starting with single-bit (full) adder for bit i
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- Prefix summation as function composition is extremely powerful!
  - Many seemingly sequential problems can be parallelized!

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= \( a + b \) (n-bit numbers)

It’s the simplest problem to demonstrate W-D tradeoffs

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- Prefix summation as function composition is extremely powerful!
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- Simple first example: binary adder – \( s = a + b \) (n-bit numbers)
  - Starting with single-bit (full) adder for bit \( i \)
But why do we care about this prefix sum so much?

\[ a \cdot a + b \cdot b \] (n-bit numbers)

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- Starting with single-bit (full) adder for bit i
- Starting with single-bit (full) adder for bit i

\[ \begin{align*}
    a_i & \rightarrow b_i \\
    c_{in,i} & \rightarrow c_{out,i} \\
    s_i & \downarrow \\
\end{align*} \]

Question: what are the functions for \( s_i \) and \( c_{out,i} \)?
But why do we care about this prefix sum so much?

\[ = aa + bb \text{ (n-bit numbers)} \]

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  - Starting with single-bit (full) adder for bit \( i \)
  
  - Starting with single-bit (full) adder for bit \( i \)

\[
\begin{align*}
\text{Question: what are the functions for } s_i \text{ and } c_{out,i}? \\
s_i &= a_i \text{ xor } b_i \text{ xor } c_{in,i} \\
c_{out,i} &= a_i \text{ and } b_i \text{ or } c_{in,i} \text{ and } (a_i \text{ xor } b_i)
\end{align*}
\]
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\end{align*}
\]

Example 4-bit ripple carry adder

Question: what are the functions for \(s_i\) and \(c_{out,i}\)?

Example 4-bit ripple carry adder source: electronics-tutorials.ws
But why do we care about this prefix sum so much?

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\end{align*}
\]

Question: what are the functions for \( s_i \) and \( c_{out,i} \)?

Show example 4-bit addition!
But why do we care about this prefix sum so much?

= \( aa + bb \) (n-bit numbers)

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- Starting with single-bit (full) adder for bit \( i \)

Question: what are the functions for \( s_i \) and \( c_{out,i} \)?

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\begin{align*}
  s_i & = a_i \text{ xor } b_i \text{ xor } c_{in,i} \\
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\end{align*}
\]

Show example 4-bit addition!

Question: what is work and depth?
Seems very sequential, can this be parallelized?

We only want $s$!
- $c_{in,2}, \ldots, c_{in,n}$ though 😊

**Carry bits can be computed with a scan!**
- Model carry bit as state starting with 0
  
  *Encode state as 1-hot vector: $q_0 = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$, $q_1 = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$*

- Each full adder updates the carry bit state according to $a_i$ and $b_i$
  
  *State update is now represented by matrix operator, depending on $a_i$ and $b_i$ ($M_{a_i b_i}$):*

  $$
  M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, \quad M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad M_{11} = \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix}
  $$

- Operator composition is defined on algebraic ring (\{0, 1, or, and\}) – i.e., replace “+” with “and” and “*” with “or”

  *Prefix sum on the states computes now all carry bits in parallel!*

**Example: $a=011, b=101 \rightarrow M_{11}, M_{10}, M_{01}$**

- Scan computes: $M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}$; $M_{11} M_{10} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}$; $M_{11} M_{10} M_{01} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}$ in parallel

- All carry states and $s_i$ can now be computed in parallel by multiplying scan result with $q_0$.
Seems very sequential, can this be parallelized?

\[ c_{in,1}, c_{in,2}, c_{in,2}, \ldots, a_i \text{ and } b_i \text{ or } c_{in,1}, \text{ and } c_{in,i} \text{ though } \]

We only want \( s \)!

- Requires \( c_{in,n}, 1 \text{ in, 1, } c_{in,2}, \ldots, c_{in,n} \) though \( \bigotimes \)

- **Carry bits can be computed with a scan!**
  - Model carry bit as state starting with 0
    - Encode state as 1-hot vector: \( q_0 = (1,0), q_1 = (0,1) \)
  - Each full adder updates the carry bit state according to \( a_i \) and \( b_i \)
    - State update is now represented by matrix operator, depending on \( a_i \) and \( b_i \) (\( M_{a_i b_i} \)):
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      M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, \quad M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}
      \]
  - Operator composition is defined on algebraic ring (\( \{0, 1, \text{or}, \text{and}\} \)) – i.e., replace “+” with “and” and “*” with “or”
    - Prefix sum on the states computes now all carry bits in parallel!

- **Example:** \( a=011, b=101 \rightarrow M_{11}, M_{10}, M_{01} \)
  - Scan computes: \( M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}; M_{11} M_{10} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}; M_{11} M_{10} M_{01} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix} \) in parallel
  - All carry states and \( s_i \) can now be computed in parallel by multiplying scan result with \( q_0 \).
Seems very sequential, can this be parallelized?

$$c_{in,1}, c_{in,2}, c_{in,2} \text{ carry bits can be computed with a scan!}$$

Carry bits can be computed with a scan!

- Model carry bit as state starting with 0
- Each full adder updates the carry bit state according to $a_i$ and $b_i$
- State update is now represented by the matrix operator, depending on $a_i$ and $b_i$ ($M_{a_i b_i}$):

$$M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, \quad M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}$$

- Operator composition is defined on an algebraic ring ($\{0, 1, \text{or, and}\}$) – i.e., replace “+” with “and” and “*” with “or”

Prefix sum on the states computes now all carry bits in parallel!

- Example: $a=011, b=101 \rightarrow M_{11}, M_{10}, M_{01}$

Scan computes:

- $M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}; M_{11} M_{10} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}; M_{11} M_{10} M_{01} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}$ in parallel

All carry states can be computed in parallel by multiplying scan result with:

$$s_i = a_i \oplus b_i \oplus c_{in,i}$$
Seems very sequential, can this be parallelized?

\[ q_0 = 1011001010 \]

We only want \( s \)!
- Requires \( c_{in}, n, 1, c_{in}, 1, c_{in}, 2 c_{in}, 2, \ldots, c_{in}, n \) though ☹

- **Carry bits can be computed with a scan!**
  - Model carry bit as state starting with 0
    - **Encode state as 1-hot vector:** \( q = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, q_1 = \begin{pmatrix} 0 \\ 1 \end{pmatrix} \)
    - **Encode state as 1-hot vector:** \( q_0 = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, q_1 = \begin{pmatrix} 0 \\ 1 \end{pmatrix} \)
  - Each full adder updates the carry bit state according to \( a_i \) and \( b_i \)
    - State update is now represented by matrix operator, depending on \( a_i \) and \( b_i \) \( (M_{a_i b_i}) \):
      \[
      M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix}
      \]
    - Operator composition is defined on algebraic ring \( \{0, 1, \text{or, and}\} \) – i.e., replace “+” with “and” and “*” with “or”
      - **Prefix sum on the states computes now all carry bits in parallel!**

- **Example:** \( a=011, b=101 \) \( \rightarrow M_{11}, M_{10}, M_{01} \)
  - Scan computes: \( M_{00} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \); \( M_{10} M_{01} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \); \( M_{11} M_0 M_{01} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \end{pmatrix} \) in parallel
Seems very sequential, can this be parallelized?

\[ M_{00} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 \end{bmatrix}, \quad M_{01} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 \end{bmatrix}, \quad M_{10} = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 \end{bmatrix}, \quad M_{11} = \begin{bmatrix} 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \]

and \( b_i b_i b_i i b_i (M a_i b_i M M M a_i b_i a_i a a a i i a_i b_i b_i b_i i b_i M a_i b_i) \): and \( b_i b_i b_i i b_i \)

\[ q_0 = 101011001010, \quad q_1 q_1 q_1 q_1 = 010100110101 \]

1 \( c_{in,1}, c_{in,2}, c_{in,n} \), \( i_{in,2}, i_{in,2}, i_{in,n} \) though ☹

We only want \( s! \)

- Requires \( c_{in,n}, 1 \ in, 1, c_{in,2}, \ldots, c_{in,n} \) though ☹

### Carry bits can be computed with a scan!

- Model carry bit as state starting with 0

\[
M_{00} = \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}, \quad M_{10} = M_{01} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad M_{11} = \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix}
\]

**Encode state as 1-hot vector:** \( q_0 = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad q_1 = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \)

- Each full adder updates the carry bit state according to \( a_i \) and \( b_i \)

State update is now represented by matrix operator, depending on \( a_i \) and \( b_i \) (\( M_{a_i b_i} \)):

\[
M_{00} = \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}, \quad M_{10} = M_{01} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad M_{11} = \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix}
\]

- Carry bits can be computed with a scan!
Seems very sequential, can this be parallelized?

\[ M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, \quad M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix} \]

and \( b_i b_i b_i b_i \) (\( M_{ai bi} MM_{ai bi} a iaa ai a i b i b b b i i b i M_{ai bi} \))

and \( b_i b_i b_i b_i \)

\[ q_0 = 101011001010, \quad q_1q_0q_11q_1 = 010100110101 \]

1 c in,1, c in,2 c in,2 i in,2 c in,2, ..., c in,n cc c in,n i in,n nn c in,n though ☹

We only want \( s! \)

- Requires \( c in, n, 1 in, 1, c in, 2, ..., c in, n \) though ☹

- Carry bits can be computed with a scan!
  - Model carry bit as state starting with 0
  - Operator composition is defined on algebraic ring \( \{0, 1, or, and\} \) – i.e., replace “+” with “and” and “*” with “or”
  - Prefix sum on the states computes now all carry bits in parallel!
  - Each full adder updates the carry bit state according to \( a_i \) and \( b_i \)

  State update is now represented by matrix operator, depending on \( a_i \) and \( b_i \) \( (M_{ai bi}) \):

\[ M_{00} = \begin{pmatrix} 1 & 1 \\ 0 & 0 \end{pmatrix}, \quad M_{10} = M_{01} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad M_{11} = \begin{pmatrix} 0 & 0 \\ 1 & 1 \end{pmatrix} \]
Seems very sequential, can this be parallelized?

\[ \begin{align*}
M_{10} &\quad MM_{10} \quad 1100 \quad M_{10} \\
0M_{00} &\quad = \quad 1100 \quad 11001110011100011001011010101101011100110000011001011011000110 \\
0101M_{01} &\quad = \quad 0110 \quad 01100011010101110100000110011010100011010000111001110011111100101101101101101111110011
\end{align*} \]

and \( \text{bibi} \text{biibi} \text{bi} \) (\( M \text{ai} \text{bi} \text{MM} \text{ai} \text{bi} \text{ai} \text{aa} \text{a} \text{ii} \text{ai} \text{bi} \text{ibi} \text{ai} \text{bi} \)):

\[ q_0 = 10 \quad 10110010 \quad 10, \quad q_1 q_2 q_3 1 = 01 \quad 01001101 \quad 01 \]

1 \( c_{in}, 1, c_{in}, 2 \quad c_{c_{in}}, 2 \quad c_{i_{in}}, 2 \quad c_{i_{in}}, ... \quad c_{in}, n \quad c_{c_{in}}, n \quad c_{i_{in}}, n \) though \( \heartsuit \)

We only want \( s \)!

- Requires \( c_{in}, n, 1 \quad in, 1, c_{in}, 2, ... , c_{in}, n \) though \( \heartsuit \)

- **Carry bits can be computed with a scan!**
  - Model carry bit as state starting with 0
  - Operator composition is defined on algebraic ring \( \{0, 1, \text{or, and}\} \) – i.e., replace “+” with “and” and “*” with “or”
    - Prefix sum on the states computes now all carry bits in parallel!
  - Each full adder updates the carry bit state according to \( a_i \) and \( b_i \)

- **Example:** \( a=011, \, b=101 \Rightarrow M_{11}, \, 11111, \, M_{10}, \, M_{01} \)

\[
\begin{align*}
M_{11} &\quad = \quad (1 \quad 1) \quad \quad M_{10} \quad = \quad (0 \quad 1) \quad \quad M_{01} \quad = \quad (0 \quad 0)
\end{align*}
\]
Seems very sequential, can this be parallelized?

\[ M_{11} = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} ; M_{10} = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \]

\[ M_{10} M_{10} M_{01} M_{01} M_{01} = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \text{ in parallel} \]

\[ M_{10} M_{00} = \begin{bmatrix} 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} , M_{10} M_{10} M_{10} M_{10} M_{10} = M_{01} M_{01} M_{01} M_{01} M_{01} = \begin{bmatrix} 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \]

and \( b_i b_i b_i i_i b_i (M_{a_i b_i} M_{a_i b_i} a_i a_i i_i a_i b_i b_i i_i b_i M_{a_i b_i}) \):

\[ q_0 = 10 1 0 1 1 0 0 1 0 1 0 , q_1 q_2 q_3 q_4 = 0 1 0 0 1 1 0 1 0 1 \]

We only want \( s \)!

- Requires \( c_i n, n, 1 i n, 1 , c_{i n, 2}, ... , c_{i n, n} \) though 😊

- **Carry bits can be computed with a scan!**
  - Model carry bit as state starting with 0
  - Operator composition is defined on algebraic ring \( \{0, 1, or, and\} \) – i.e., replace “+” with “and” and “*” with “or”
  - Prefix sum on the states computes now all carry bits in parallel!
Seems very sequential, can this be parallelized?

can now be computed in parallel by multiplying scan result \( q_0 \) by \( q \).

\[
1 M_{11} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} ;
\]

\[
10 M_{10} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} ;
\]

\[
M_{10} M_{10} M_{10} 1100 M_{10} , M_{01} M_{11} M_{01} 0011 M_{01}
\]

\[
0 M_{00} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 1 \\ 1 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} ;
\]

and \( bbbbibi ( M a i b i M M M a i b i a i a a a i i a i b i b b i i i b i M a i b i ) : \)

and \( bbbbibi \)

\[
q 0 = 10 10110010 10 , q 1 q q q 1 1 q 1 = 01 01001101 01
\]

We only want \( s \)!

- Requires \( c i n , n , 1 i n , 1 , c i n , 2 , ... , c i n , n \) though \( \oplus \)

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Prefix sums as magic bullet for other seemingly sequential algorithms

Any time a sequential chain can be modeled as function composition!

- \( f_0, \ldots, f_n \) be an ordered set of functions and \( f_0(x) = x \)
- Define ordered function compositions: \( f_1(x); f_2(f_1(x)); \ldots; f_n(f_{n-1}(x)) \)
- If we can write function composition \( g(x) = f_i(f_{i-1}(x)) \) as \( g = f_i \circ f_{i-1} \) then we can compute \( \circ \) with a prefix sum!

\( \text{We saw an example with the adder (} M_{ab} \text{ were our functions) } \)

- Example: linear recurrence \( f_i(x) = a_i f_{i-1}(x) + b_i \) with \( f_0(x) = x \)
  - Write as matrix form \( f_i(x) = \begin{pmatrix} a_i & b_i \\ 0 & 1 \end{pmatrix} f_{i-1}(x) \)
  - Function composition is now simple matrix multiplication!

\( \text{For example: } f_2(x) = \begin{pmatrix} a_2 & b_2 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} a_1 & b_1 \\ 0 & 1 \end{pmatrix} f_0(x) = \begin{pmatrix} a_1a_2 & a_2b_1 + b_2 \\ 0 & 1 \end{pmatrix} x \)

- Most powerful! Homework:
  - Parallelize tridiagonal solve
  - Parallelize string parsing
Prefix sums as magic bullet for other seemingly sequential algorithms

\[ f_1, \ldots, f_n, f_0 \] be an ordered set of functions and \( f_0 f f f 0 f 0 f 0 x x x x = x x \)

Any time a sequential chain can be modeled as function composition!

- Let \( f_1, f_2, \ldots, f_n \) be an ordered set of functions and \( f_0(x) = x \)
- Define ordered function compositions: \( f_1(x); f_2(f_1(x)); \ldots; f_n(... f_1(x)) \)
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  - Parallelize tridiagonal solve
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Prefix sums as magic bullet for other seemingly sequential algorithms

\[ f_1(x); f_2(x); f_2(x); f_2(x); f_2(x); \ldots; f_n(x); f_n(x); f_n(x); \ldots f_n(x); \ldots f_1(x); x \times f_1(x) \]

\[ f_1, \ldots, f_n \text{ be an ordered set of functions and } f_0(f_0(x)) = x \]

Any time a sequential chain can be modeled as function composition!

- Define ordered function compositions: \( f_1(x); f_2(f_1(x)); \ldots; f_n(... f_1(x)) \)
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  For example:
  
  \[ f_2(x) = \begin{pmatrix} a_2 & b_2 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} a_1 & b_1 \\ 0 & 1 \end{pmatrix} f_0(x) = \begin{pmatrix} a_1 a_2 & a_2 b_1 + b_2 \\ 0 & 1 \end{pmatrix} (x) \]

- **Most powerful!** Homework:
  - Parallelize tridiagonal solve
Prefix sums as magic bullet for other seemingly sequential algorithms

were our functions)

\[ f(x) = f(i-1) f f f i-1 \ (f \ i i g x) = f (f -1) f f f i i i f i \ i i f i \ i i f i -1 f f f i -1 \ i i -1 f i -1 \]

then we can compute \( \circ \) with a prefix sum!

\[ f \ 1 \ (x x): f 2 f f 2 2 f 2 (f 1 f f 1 1 f 1 x x x); \ldots; f n f f n n n n f n (f 1 f f 1 1 f 1 x x x) \]

\[ f 1, \ldots, f n f f f n n n f n \]

be an ordered set of functions and \( f 0 f f 0 f 0 x x x = x x \)

Any time a sequential chain can be modeled as function composition!

We saw an example with the adder (\( M ab\ ab b ab \) were our functions)

- Define ordered function compositions: \( f_1(x); f_2(f_1(x)); \ldots; f_n(\ldots f_1(x)) \)
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Prefix sums as magic bullet for other seemingly sequential algorithms

\[
\begin{align*}
   a i & \quad a i i i a i f i-1 f f f i-1 i i-1 f i-1 x x x x + b i b b i i b i i \quad \text{with} \quad f 0 f f f 0 0 f 0 x x x x = x \\
   f f g x = f i i i g x = f i (f i-1 f f f i-1 i i-1 f i-1 x x x x) \quad \text{as} \quad g g = f i f f i i f i \circ f i-1 f f f i-1 i i-1 f i-1 \\
   \text{then we can compute} \circ \text{with a prefix sum!} \\
   f 1(x x); \ f 2 f f f 2 2 f 2 (f 1 f f f 1 1 f 1 x x x x); \ ... \ ; \ f n f f f n n n f n (... f 1 f f f 1 1 f 1 x x x x) \\
   \ f 1 , ..., f n f f f n n n f n \ \text{be an ordered set of functions and} \ f 0 f f f 0 0 f 0 x x x x = x x
\end{align*}
\]

Any time a sequential chain can be modeled as function composition!

We saw an example with the adder (\( M a b \ a b b a b \) were our functions)

- **Example: linear recurrence** \( f i x = i i i i(x) = a_i f_{i-1}(x) + b_i \) with \( f_0(x) = x \)
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- **Example: linear recurrence** \( f_i(x) = a_i f_{i-1}(x) + b_i \) with \( f_0(x) = x \)
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  - Function composition is now simple matrix multiplication!

For example:

\[
\begin{align*}
   a & = \begin{pmatrix} 1 & 1 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} a_i \\ b_i \end{pmatrix} \\
   b & = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \begin{pmatrix} a_i \\ b_i \end{pmatrix} 
\end{align*}
\]

Prefix sums as magic bullet for other seemingly sequential algorithms
Prefix sums as magic bullet for other seemingly sequential algorithms

\[ x_1 \cdot x_1 = a_i b_i 0 1 \ a_i b_i 0 1 a_i a a a i i a i \ a_i b_i 0 1 b_i b_i b_i i i b_i a_i b_i 0 1 \\
1 a_i b_i 0 1 a_i b_i 0 1 f_i-1 f f_i-1 i i-1 f_i-1 x_1 x_1 x x 1 1 x_1 x_1 \]

\[ a_i a a a i i a i f_i-1 f f_i-1 i i-1 f_i-1 x x x + b_i b_i b_i i i b_i \] with \( f_0 f f_0 0 0 f_0 x x x = x \)

were our functions)

\[ f f g x = f i i g x = f i (f_i-1 f f_i-1 i i-1 f_i-1 x x x x) \] as \( g g = f_i f f_i i i f_i \circ f_i-1 f f_i-1 i i-1 f_i-1 \)

then we can compute \( \circ \) with a prefix sum!

\[ f_1 (x x); \ f_2 f f_2 2 f_2 (f_1 f f_1 1 f_1 x x x x); \ldots; \ f_n f f_n n n f_n (\ldots f_1 f f_1 1 f_1 x x x x) \]

\[ f_1, \ldots, \ f_n f f_n n n f_n \] be an ordered set of functions and \( f_0 f f_0 0 f_0 x x x = x x \)

*Any time a sequential chain can be modeled as function composition!*

  We saw an example with the adder (\( M \ a b \ a b \ b a b \) were our functions)

- Write as matrix form \[ f \ i \ x 1 1 1 x 1 i i i (x) = \begin{pmatrix} a_i \\ b_i \end{pmatrix} f_{i-1} (x) \]
- If we can write function composition \( g(x) = f_i(f_{i-1}(x)) \) as \( g = f_i \circ f_{i-1} \) then we can compute \( \circ \) with a prefix sum!

  We saw an example with the adder (\( M_{ab} \) were our functions)

- **Example: linear recurrence** \( f_i(x) = a_i f_{i-1}(x) + b_i \) with \( f_0(x) = x \)

Prefix sums as magic bullet for other seemingly sequential algorithms
Prefix sums as magic bullet for other seemingly sequential algorithms

\[ f 2 \ x 1 \ x 1 xx x 1 1 x 1 \ x 1 = a 2 \ b 2 0 1 \ a 2 \ b 2 0 1 \ a 2 aa a 2 a 2 \ a 2 \ b 2 0 1 \ b 2 b b b 2 2 b 2 a 2 b 2 0 1 0 a 2 b 2 0 1 0 a 2 b 2 0 1 a 1 b 1 0 1 a 1 b 1 0 1 a 1 a a 1 1 a 1 a 1 b 1 0 1 b 1 0 1 1 a 1 b 1 0 1 f 0 f f f 0 f 0 f 0 x 1 x 1 xx x 1 1 x 1 x 1 = a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a a a 1 1 a 1 a 2 aa a 2 2 a 2 a 1 a 2 a 2 b 1 + b 2 0 1 a 2 b 1 a 2 a a a 2 2 a b b a 2 b 1 + b 2 b b b 2 2 b 2 a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a 2 a 2 b 1 + b 2 0 1 x 1 x 1 xx x 1 1 x 1 \\

x 1 x 1 = a i b i 0 1 a i b i 0 1 a i a a a i i a i a i b i 0 1 b i b b b i i b i a i b i 0 1 a i b i 0 1 a i b i 0 1 f i - 1 f f f i - 1 i i - 1 f i - 1 x 1 x 1 xx x 1 1 x 1 a i a a a i i a i f i - 1 f f f i - 1 i i - 1 f i - 1 x x x + b i b b b i i b i \text{ with } f 0 f f f 0 f 0 f 0 x x x = x \text{ were our functions) }

f f g x = f i i g x = f i ( f i - 1 f f f i - 1 i i - 1 f i - 1 x x x ) \text{ as } g g = f i f f f i i f i \circ f i - 1 f f f i - 1 i i - 1 f i - 1 \text{ then we can compute } \circ \text{ with a prefix sum! }

f 1 (x x) ; f 2 f f f 2 2 f 2 ( f 1 f f f 1 1 f 1 x x x ) ; \ldots ; f n f f f n n n f n ( f 1 f f f 1 1 f 1 x x x ) = f 1 , , , \ldots , f n f f f n n n f n \text{ be an ordered set of functions and } f 0 f f f 0 f 0 f 0 x x x = x x

Any time a sequential chain can be modeled as function composition!

- We saw an example with the adder ( M a b , a b b , a b were our functions)
Prefix sums as magic bullet for other seemingly sequential algorithms

\[
f 2 \ x 1 \ x 1 x x x 1 1 x 1 \ x 1 = a 2 \ b 2 0 1 \ a 2 \ b 2 0 1 \ a 2 a a a 2 a 2 \ a 2 \ b 2 0 1 b 2 b b b 2 2 b 2 a 2 \ b 2 0 1 0 a 2 \ b 2 0 1 1 a 2 b 2 0 1 a 1 b 1 0 1 a 1 b 1 0 1 a 1 a a a 1 1 a 1 a 1 b 1 0 1 b 1 0 1 0 a 1 b 1 0 1 f 0 f f 0 0 f 0 x 1 \ x 1 x x x 1 1 x 1 x 1 = a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a a a 1 1 a 1 a 2 a a a a 2 2 a 2 a 1 a 2 a 2 b 1 + b 2 0 1 a 2 b 1 a 2 a a a 2 a 2 b b a 2 b 1 + b 2 b b b 2 2 b 2 a 1 a 2 a 2 b 1 + b 2 0 1 a 1 a 2 a 2 b 1 + b 2 0 1 1 a 1 x 1 x x x 11 x 1 x 1 a i a a a i i a i a i b i 0 1 a i b i 0 1 f i − 1 f f f i − 1 i i − 1 f i − 1 x 1 x 1 x x x 11 x 1 x 1 a i a a a i i a i f i − 1 f f f i − 1 i i − 11 f i − 1 x x x + b i b b b i i b i \text{ with } f 0 f f f 0 0 0 f 0 x x x = x \text{ were our functions)}
\]

\[
ff g x = f i i g x = f i \left(f i − 1 f f f i − 1 i i − 1 f i − 1 x x x \right) \text{ as } gg = f i f f f i i f i \circ f i − 1 f f f i − 1 i i − 1 f i − 1 \text{ then we can compute } \circ \text{ with a prefix sum!}
\]

\[
f 1 (x x); f 2 f f f 2 2 f 2 \left(f 1 f f f 1 1 f 1 x x x \right) ; \ldots ; f n f f f n n n f n \left(\ldots f 1 f f f 1 1 f 1 x x x \right) \]

\[
f 1 , \ldots , f n f f f n n n f n \text{ be an ordered set of functions and } f 0 f f f 0 0 f 0 x x x = x x
\]

Any time a sequential chain can be modeled as function composition!

We saw an example with the adder (\(M_{ah}, ah, ah\) were our functions)
Prefix sums as magic bullet for other seemingly sequential algorithms

\[
\begin{align*}
&f_1(x), f_2 f f f 22 f_2 (f_1 f f f 11 f_1 x x x); \ldots; f n f f n n n f n (f_1 f f f 11 f_1 x x x) \\
&f_1, \ldots, f n f f n n n f n \text{ be an ordered set of functions and } f 0 f f f 0 f 0 x x x = x x
\end{align*}
\]

*Any time a sequential chain can be modeled as function composition!*

We saw an example with the adder \((M_{ab}, ab \cdot ah, ah)\); were our functions)
Another use for prefix sums: Parallel radix sort

- stably sort all values by the $i$-th bit
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - stably sort all values by the $i$-th bit
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts k-bit numbers in k iterations
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Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts k-bit numbers in k iterations
  - In each iteration $i$ stably sort all values by the $i$-th bit
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts $k$-bit numbers in $k$ iterations
  - In each iteration $i$ stably sort all values by the $i$-th bit
  - Example, $k=1$:
    
    \[
    \text{Iteration 0: 101 111 010 011 110 001}
    \]
Another use for prefix sums: Parallel radix sort

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    *Iteration 1*: 010 110 101 111 011 001
Another use for prefix sums: Parallel radix sort

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  - Example, $k=1$:
    
    Iteration 0: 101 111 010 011 110 001
    Iteration 1: 010 110 101 111 011 001
    Iteration 2: 101 001 010 110 111 011
Another use for prefix sums: Parallel radix sort

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  - Example, $k=1$:
    - Iteration 0: 101 111 010 011 110 001
    - Iteration 1: 010 110 101 111 011 001
    - Iteration 2: 101 001 010 110 111 011
    - Iteration 3: 001 010 011 101 110 111
Another use for prefix sums: Parallel radix sort

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    **Iteration 0:** 101 111 010 011 110 001
    
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    **Iteration 2:** 101 001 010 110 111 011
    
    **Iteration 3:** 001 010 011 101 110 111

- Now on $n$ processors
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts $k$-bit numbers in $k$ iterations
  - In each iteration $i$ stably sort all values by the $i$-th bit
  - Example, $k=1$:
    
    Iteration 0: 101 111 010 011 110 001
    Iteration 1: 010 110 101 111 011 001
    Iteration 2: 101 001 010 110 111 011
    Iteration 3: 001 010 011 101 110 111

- Now on $n$ processors
  - Each processor owns single $k$-bit number, each iteration
Another use for prefix sums: Parallel radix sort

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    Iteration 1: 010 110 101 111 011 001
    Iteration 2: 101 001 010 110 111 011
    Iteration 3: 001 010 011 101 110 111
  
- Now on $n$ processors
  - Each processor owns single k-bit number, each iteration
    
    $low = prefix\_scan(!bit, sum)$
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts k-bit numbers in k iterations
  - In each iteration $i$ stably sort all values by the $i$-th bit
  - Example, k=1:
    
    Iteration 0: 101 111 010 011 110 001
    Iteration 1: 010 110 101 111 011 001
    Iteration 2: 101 001 010 110 111 011
    Iteration 3: 001 010 011 101 110 111

- Now on n processors
  - Each processor owns single k-bit number, each iteration
    
    low = prefix_scan(!bit, sum)
    high = n-1-backwards_prefix_scan(bit, sum)
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
  - Sorts k-bit numbers in k iterations
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    Iteration 1: 010 110 101 111 011 001
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    Iteration 3: 001 010 011 101 110 111

- Now on $n$ processors
  - Each processor owns single $k$-bit number, each iteration
    
    $\text{low} = \text{prefix\_scan}(!\text{bit}, \text{sum})$
    
    $\text{high} = n-1\text{-backwards\_prefix\_scan}(\text{bit}, \text{sum})$
    
    $new\_idx = (\text{bit} == 0) : \text{low} ? \text{high}$
Another use for prefix sums: Parallel radix sort

- **Radix sort works bit-by-bit**
  - Sorts k-bit numbers in k iterations
  - In each iteration \( i \) stably sort all values by the \( i \)-th bit
  - Example, \( k=1 \):
    - **Iteration 0**: 101 111 010 011 110 001
    - **Iteration 1**: 010 110 101 111 011 001
    - **Iteration 2**: 101 001 010 110 111 011
    - **Iteration 3**: 001 010 011 101 110 111

- **Now on n processors**
  - Each processor owns single k-bit number, each iteration
    - \( \text{low} = \text{prefix\_scan}(!\text{bit, sum}) \)
    - \( \text{high} = n-1\text{-backwards\_prefix\_scan(\text{bit, sum})} \)
    - \( \text{new\_idx} = (\text{bit} == 0) : \text{low} \ ? \text{high} \)
    - \( b[\text{new\_idx}] = a[i] \)
    - \( \text{swap}(a,b) \)
Another use for prefix sums: Parallel radix sort

- **Radix sort works bit-by-bit**
  - Sorts k-bit numbers in k iterations
  - In each iteration \( i \) stably sort all values by the \( i \)-th bit
  - Example, \( k=1 \):
    
    - **Iteration 0:** 101 111 010 011 110 001
    - **Iteration 1:** 010 110 101 111 011 001
    - **Iteration 2:** 101 001 010 110 111 011
    - **Iteration 3:** 001 010 011 101 110 111

- **Now on \( n \) processors**
  - Each processor owns single k-bit number, each iteration
    
    \[
    \begin{align*}
    \text{low} &= \text{prefix\_scan}(!\text{bit, sum}) \\
    \text{high} &= \text{n-1-backwards\_prefix\_scan}(\text{bit, sum}) \\
    \text{new\_idx} &= (\text{bit} == 0) : \text{low} ? \text{high} \\
    \text{b[new\_idx]} &= \text{a[i]} \\
    \text{swap(a,b)}
    \end{align*}
    \]

  Show one example iteration!
Another use for prefix sums: Parallel radix sort

- Radix sort works bit-by-bit
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- Now on $n$ processors
  - Each processor owns single k-bit number, each iteration
    
    ```
    low = prefix_scan(!bit, sum)
    high = n-1-backwards_prefix_scan(bit, sum)
    new_idx = (bit == 0) : low ? high
    b[new_idx] = a[i]
    swap(a,b)
    ```
  
  Show one example iteration!
  
  Question: work and depth?
Oblivious graph algorithms

- Seems paradoxical but isn’t (may just not be most efficient)
  - Use adjacency matrix representation of graph – “compute with all zeros”
Oblivious graph algorithms

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Unweighted graph – binary matrix
Oblivious graph algorithms

- Seems paradoxical but isn’t (may just not be most efficient)
  - Use adjacency matrix representation of graph – “compute with all zeros”

Unweighted graph – binary matrix

Weighted graph – general matrix
Algebraic semirings

A semiring is an algebraic structure that

\( (\times, +, 0, 1) \)

Boolean semiring: \((\{0,1\}, \lor, \land, 0, 1)\)

Tropical semiring: \((\mathbb{R} \cup \{\infty\}, \min, +, \infty, 0)\) (also called min-plus semiring)
Algebraic semirings

A semiring is an algebraic structure that

- Has two binary operations called “addition” and “multiplication”

, +, *, 0, 1)

Boolean semiring: ({0,1}, ∨, ∧, 0, 1)

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Algebraic semirings

A semiring is an algebraic structure that

- Has two binary operations called "addition" and "multiplication"
- Addition must be associative \(((a+b)+c = a+(b+c))\) and commutative \((a+b=b+a)\) and have an identity element

\(\{+, \ast, 0, 1\}\)

*Boolean semiring: \(\{0,1\}, \lor, \land, 0, 1\)*

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$(+, *, 0, 1)$

Boolean semiring: $\{0,1\}, \lor, \land, 0, 1$

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- Semirings are denoted by tuples \((S, +, *, 0, 1)\)

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“Standard” ring of rational numbers: \((\mathbb{R}, +, *, 0, 1)\)

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Algebraic semirings

\( \cup \{\infty\}, \ min, +, \ \infty, \ 0 \) (also called min-plus semiring)

\( \wedge, \ 0, 1 \)

\( \cup, +, *, \ 0, 1 \)

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Tropical semiring: \((\mathbb{R} \cup \{\infty\}, \ min, +, \infty, 0)\) (also called min-plus semiring)
Oblivious shortest path search

\[
\begin{array}{ccccccc}
0 & 2 & 3 & \infty & \infty & \infty & \infty \\
\infty & 0 & \infty & \infty & 3 & 1 & \\
\infty & \infty & 0 & \infty & \infty & 2 & \\
\infty & \infty & 4 & 0 & \infty & \infty & \\
\infty & \infty & \infty & 7 & 0 & \infty & \\
\infty & \infty & \infty & \infty & 8 & 0 & \\
\end{array}
\]
Oblivious shortest path search

- Construct distance matrix from adjacency matrix by replacing all off-diagonal zeros with $\infty$
Oblivious shortest path search

- Construct distance matrix from adjacency matrix by replacing all off-diagonal zeros with $\infty$
Oblivious shortest path search

- f size n to \( \infty \) everywhere but zero at start vertex
- Initialize distance vector \( d_0 \) of size n to \( \infty \) everywhere but zero at start vertex
Oblivious shortest path search

- $\infty, 0, \infty, \infty, 0 \rightarrow T \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, \infty, 0, \infty, 0\rightarrow T$
- f size n to $\infty$ everywhere but zero at start vertex

Show evolution when multiplied!
Oblivious shortest path search

- ∞, 0,∞, ∞, ∞, ∞, ∞ T ∞, 0,∞, ∞, ∞, ∞, ∞, 0,∞, ∞, ∞, ∞, 0,∞, ∞, ∞, ∞, 0,∞, ∞, 0,∞, ∞, ∞, 0,∞, ∞, ∞, ∞, ∞, ∞, ∞, 0,∞, ∞, ∞, ∞, ∞ ∞, 0,∞, ∞, ∞, ∞, ∞ T

- f size n to ∞ everywhere but zero at start vertex

- Show evolution when multiplied!

- SSSP can be performed with n+1 matrix-vector multiplications!
Oblivious shortest path search

- $\infty, 0, \infty, \infty, \infty, \infty \ T \infty, 0, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty \ T$
- $f$ size $n$ to $\infty$ everywhere but zero at start vertex
- 
  Show evolution when multiplied!

- SSSP can be performed with $n+1$ matrix-vector multiplications!
  - Question: total work and depth?
Oblivious shortest path search

- $O(n^3 \cdot n^3 \cdot n^3)$, $DD = O(n \cdot n \cdot \log n)$
- $\infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty

- f size n to $\infty$ everywhere but zero at start vertex

- Show evolution when multiplied!

- SSSP can be performed with $n+1$ matrix-vector multiplications!
  - Question: total work and depth?
    - $W = O(n^3)$, $D = O(n \cdot \log n)$
Oblivious shortest path search

- $O(O(n^3 n^3 n^3 n^3), DD=O(n n \log n))$
- $0, \infty, 0, \infty, 0, 0, \infty, 0, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, T, T, T, T$
- $f$ size $n$ to $\infty$ everywhere but zero at start vertex

Show evolution when multiplied!

SSSP can be performed with $n+1$ matrix-vector multiplications!
- Question: total work and depth?
- Question: Is this good? Optimal?
Oblivious shortest path search

- $E \in \mathbb{E} \in \mathbb{E} + V V V V \log V V V V$
- $O(\, n 3 \, n n \, n 3 \, n 3 \, n 3 \,) \), $DD=O(n n \log n n)$
- $\infty, 0, \infty, \infty, \infty, \infty, T \infty, 0, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, T$
- $f \text{ size } n \text{ to } \infty \text{ everywhere but zero at start vertex}$

Show evolution when multiplied!

- **SSSP can be performed with** $n+1 \text{ matrix-vector multiplications!}$
  - Question: total work and depth?
  - Question: Is this good? Optimal?
  - *Dijkstra* = $O(|E| + |V| \log |V|)$
Oblivious shortest path search

- \( O_O( n 3 \, n n \, n 3 \, n 3 \, n 3 \, n \log n n ) \)
- \( DD = O_O( \log 2 \log 2 \, 2 \log 2 \, n n ) \)
- \( E = E E E + V V V V \log V V V V \)
- \( O_O( n 3 \, n n \, n 3 \, n 3 \, n 3 ) \), \( DD = O_O( n n \log n n ) \)
- \( \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, 0, \infty, \infty, \infty, \infty, \infty, \infty, \infty, \infty, T \)

- \( f \) size \( n \) to \( \infty \) everywhere but zero at start vertex

- Show evolution when multiplied!

SSSP can be performed with \( n + 1 \) matrix-vector multiplications!
- Question: total work and depth?
- Question: Is this good? Optimal?

\( \text{Dijkstra} = O( |E| + |V| \log |V| ) \)

Homework:
- Define a similar APSP algorithm with

\( W = O(n^3 \log n) \), \( D = O(\log^2 n) \)
Oblivious connected components

Question: How could we compute the transitive closure of a graph?

- \((A + I)^n\) times with itself in the Boolean semiring!
- Why?
  
  *Demonstrate that \((A + I)^2\) has 1s for each path of at most length 1
  *By induction show that \((A + I)^k\) has 1s for each path of at most length \(k\)

- What is work and depth of transitive closure?
  - Repeated squaring! \(W = O(n^3 \log n)\) \(D = O(\log^2 n)\)

- How to get to connected components from a transitive closure matrix?
  - Each component needs unique label
  - Create label matrix \(L_{ij} = j\) iff \((A_I)^n_{ij} = 1\) and \(L_{ij} = \infty\) otherwise
  - For each row (vertex) perform min-reduction to determine its component label!
  - Overall work and depth?
    \(W = O(n^3 \log n), D = O(\log^2 n)\)
Oblivious connected components

Question: How could we compute the transitive closure of a graph?

- \( A + I \) \( n \) times with itself in the Boolean semiring!
- Why?
  
  \[ (A + I)^2 \] has 1s for each path of at most length 1
  
  By induction show that \( (A + I)^k \) has 1s for each path of at most length \( k \)

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  - Overall work and depth?
    
    \[ W = O(n^3 \log n), D = O(\log^2 n) \]
Oblivious connected components

\((A + I)n)\) times with itself in the Boolean semiring!

**Question:** How could we compute the transitive closure of a graph?

- Multiply the matrix \((A + I)\) \(n\) times with itself in the Boolean semiring!
- Why?

  *Demonstrate that \((A + I)^2\) has 1s for each path of at most length 1*
  
  *By induction show that \((A + I)^k\) has 1s for each path of at most length \(k\)*

**What is work and depth of transitive closure?**

- Repeated squaring! \(W = O(n^3 \log n), D = O(\log^2 n)\)

**How to get to connected components from a transitive closure matrix?**

- Each component needs unique label
- Create label matrix \(L_{ij} = j\) iff \((A_I)^n_{ij} = 1\) and \(L_{ij} = \infty\) otherwise
- For each row (vertex) perform min-reduction to determine its component label!
- Overall work and depth?

\(W = O(n^3 \log n), D = O(\log^2 n)\)
Oblivious connected components

\[ A + I \ 2 \ 2 \ A + I \ 2 \] has 1s for each path of at most length 1
\[ AA + II \] times with itself in the Boolean semiring!

Question: How could we compute the transitive closure of a graph?

- Why?
  
  Demonstrate that \( A + I \ 2 \) has 1s for each path of at most length 1
  
  Demonstrate that \( (A + I)^2 \) has 1s for each path of at most length 1
  
  By induction show that \( (A + I)^k \) has 1s for each path of at most length \( k \)

- What is work and depth of transitive closure?
  
  Repeated squaring! \( W = O(n^3 \log n) \) \( D = O(\log^2 n) \)

- How to get to connected components from a transitive closure matrix?
  
  Each component needs unique label
  
  Create label matrix \( L_{ij} = j \) iff \( (A_i)^n \) \( i \) \( = j \) and \( L_{ij} = \infty \) otherwise
  
  For each row (vertex) perform min-reduction to determine its component label!
  
  Overall work and depth?
Oblivious connected components

$I A + I A + I k k k A + I k$ has 1s for each path of at most length $k$

$I A + I A + I 2 2 2 A + I 2$ has 1s for each path of at most length 1

$A A + I I n n$ times with itself in the Boolean semiring!

Question: How could we compute the transitive closure of a graph?

- Why?
  
  By induction show that $A + I A + I k$ has 1s for each path of at most length $k$
  
  Demonstrate that $(A + I)^2$ has 1s for each path of at most length 1
  
  By induction show that $(A + I)^k$ has 1s for each path of at most length $k$

- What is work and depth of transitive closure?
  
  - Repeated squaring! $W = O(n^3 \log n)$ $D = O(\log^2 n)$

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  - For each row (vertex) perform min-reduction to determine its component label!
Oblivious connected components

\[ A + I \ A + I \ k \ k \ A + I \ k \text{ has 1s for each path of at most length } k \]
\[ A + I \ A + I \ 2 \ 2 \ A + I \ 2 \text{ has 1s for each path of at most length } 1 \]
\[ AA + II \] \( n \) times with itself in the Boolean semiring!

Question: How could we compute the transitive closure of a graph?

- Why?
  - By induction show that \( A + I \ A + I \ k \text{ has 1s for each path of at most length } k \)

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Oblivious connected components

\[ O(n^3 \log n) \quad DD = OO(\log 2 \log 2 \log 2 \log 2 \log 2 n) \]

II \( A+I \quad A+I \quad k \quad k \quad A+I \quad k \) has 1s for each path of at most length \( k \)

II \( A+I \quad A+I \quad 2 \quad 2 \quad A+I \quad 2 \) has 1s for each path of at most length 1

AA+II) nn times with itself in the Boolean semiring!

Question: How could we compute the transitive closure of a graph?

- Why?
  
  By induction show that \( A + I \quad A + I \quad k \) has 1s for each path of at most length \( k \)

- What is work and depth of transitive closure?
  
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- What is work and depth of transitive closure?
  
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  Each component needs unique label
  
  Create label matrix \( L_{ij} = j \) iff \( (A_I)^n \)
  
  \( L_{ij} = 1 \) and \( L_{ij} = \infty \) otherwise
**Oblivious connected components**

\[ O(n^3 n n 3 n 3 n 3 \log n n) \] \[ D D = O(n^3 \log 2 \log 2^2 \log 2 n n) \]

II \( A + I \) \( A + I \ k k k \ A + I \ k \) has 1s for each path of at most length \( k \)

II \( A + I \) \( A + I \ 2 2 A + I \ 2 \) has 1s for each path of at most length \( 1 \)

\( AA + II \) \( n n \) times with itself in the Boolean semiring!

**Question:** How could we compute the transitive closure of a graph?

- **Why?**
  
  *By induction show that* \( A + I A + I k \) has 1s for each path of at most length \( k \)

- **What is work and depth of transitive closure?**
  
  - Repeated squaring! \( W = O(n^3 \log n) \) \( D = O(\log^2 n) \)

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Oblivious connected components

\[ O(n^3 \log n) \] \[ DD = O(n^2 \log n) \]

Why?
- By induction show that \( A + I \) \( A + I \) \( k \) has 1s for each path of at most length \( k \)
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Question: How could we compute the transitive closure of a graph?

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Oblivious connected components

\[
jj \text{ iff } A I n ij \ A I n A I A I A I A I A I A I n n n A I n A I n ij ij j A I n
\]
\[
i ij l ij = \infty \text{ otherwise}
\]

\[
OO( n 3 n 3 n 3 n 3 \log nn) DD = OO( \log 2 \log 2 \log 2 \log 2 \log 2 \log nn)
\]

\[
II A+I A+I k kk A+I k \text{ has } 1s \text{ for each path of at most length } k
\]

\[
II A+I A+I 2 2 A+I 2 \text{ has } 1s \text{ for each path of at most length } 1
\]

\[
AA+II) nn \text{ times with itself in the Boolean semiring!}
\]

Question: How could we compute the transitive closure of a graph?

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- How to get to connected components from a transitive closure matrix?
Oblivious connected components

\[ jj \text{ iff } AI n ij AI n AI A I A A A I II AI AI n nn AI n AI n j j i j j i i j L i j = \infty \text{ otherwise} \]

\[ O0( n 3 nn n 3 3 n 3 \log nn) DD=O0( \log 2 \log 2 2 2 \log 2 \log 2\, nn) \]

\[ II A+I A+I k\, kk A+I k \text{ has 1s for each path of at most length } k \]

\[ II A+I A+I 2 2 A+I 2 \text{ has 1s for each path of at most length } 1 \]

\[ AA+II) nn \text{ times with itself in the Boolean semiring!} \]

**Question:** How could we compute the transitive closure of a graph?

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  By induction show that \( A+I A+I k \) has 1s for each path of at most length \( k \)

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Oblivious connected components

\[ jj \text{ iff } A I n ij \quad A I n A I A I A A A I I I A I A I A I n nn A I n A I n ij iijj A I n iiijj L ij = \infty \text{ otherwise} \]

\[ OO( n 3 nn n 3 n 3 n 3 \log nn) \quad DD = OO( \log 2 \log 2 \log 2 \log 2 \log 2 nn) \]

\[ II A + I \quad A + I k k k A + I k \quad \text{has} \ 1s \ \text{for each path of at most length} \ k \]

\[ II A + I A + I 2 2 A + I 2 \quad \text{has} \ 1s \ \text{for each path of at most length} \ 1 \]

\[ AA + II) nn \quad \text{times with itself in the Boolean semiring!} \]

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  By induction show that \( A + I A + I k \) has 1s for each path of at most length \( k \)

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  - Repeated squaring! \( W = O(n^3 \log n) \) \( D = O(\log^2 n) \)

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- **Now moving to non-oblivious 😊**