DPHPC: Amdahl’s Law, Roofline model

Recitation session
Why do we have to do performance modelling?

• Will my program scale?
  “Am I going to run faster on twice larger machine?”

• Which parts of the program I should improve?
  “Let me parallelize one more loop, that should help… I can't be spending 90% of time on communication and synchronization!”

• Can my program achieve better performance? How far is it from maximum?
  “I spent 50 hours on optimizing every memory accesses and I’m 0.5% faster”

• How should we design a new computing system?
  “Do I need accelerators? Do I need more memory?”
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Two things we need to understand

• Baseline – slow and bad programs tend to scale better.
• Upper bound
Why is upper bound important?

This is pretty pathetic…
Why is upper bound important?
Why is upper bound important?

Upper bound for prefix scan
Why is upper bound important?

Upper bound for prefix scan

We’re actually improving!
Amdahl’s Law

Time of sequential program with f as the fraction not affected by the parallelization:

\[ T_1 = fT_1 + (1 - f)T_1 \]
Amdahl’s Law

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Time of parallel program:

$$T_P \geq fT_1 + \frac{(1 - f)T_1}{P}$$
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Speedup:

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S_P = \frac{T_1}{T_P} \leq \frac{1}{\frac{1}{P} + f}
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S_P = \frac{T_1}{T_P} \leq \frac{1}{1 - f_P + f}
\]

Possible factors: load balancing, communication costs, I/O, scheduling

It’s like to see the glass as half empty but…

It could be even worse!

Serial work

Parallelizable work

Sp

Number of processors
Amdahl’s Law vs Gustafson-Barsis' Law

...speedup should be measured by scaling the problem to the number of processors, not by fixing the problem size.
— John Gustafson
Amdahl’s Law vs Gustafson-Barsis' Law

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Time of sequential program with $\alpha$ as the fraction not affected by the parallelization on P-processors machine:

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Speedup:

$$S_P = \frac{T_1}{T_P} \leq \alpha + P(1 - \alpha)$$
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Note: no parallel overheads are taken into account here!
Quiz

• Speedup

• Efficiency

• Strong Scaling

• Weak Scaling
Quiz

• Speedup
  ▪ How well something responds to adding more resources
  ▪ **What’s your base case?** The best serial version or a single parallel process?

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  ▪ How well something responds to adding more resources
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• Efficiency
  ▪ Gives idea on the “utilization” degree of the computing resources

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  ▪ Problem size stays fixed as the number of processing elements are increased

• Weak Scaling

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Exercise 1

Assume 1% of the runtime of a program is not parallelizable. This program is run on 61 cores of an Intel Xeon Phi. Under the assumption that the program runs at the same speed on all of those cores, and there are no additional overheads, what is the parallel speedup?
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Amdahl’s law assumes that a program consists of a serial part and a parallelizable part. The fraction of the program which is serial can be denoted as $B$ — so the parallel fraction becomes $1 - B$. If there is no additional overhead due to parallelization, the speedup can therefore be expressed as

$$S(n) = \frac{1}{B + \frac{1}{n}(1 - B)}$$

For the given value of $B = 0.01$ we get $S(61) = 38.125$. 
Exercise 2

Assume 0.1% of the runtime is not parallelizable. The program also invokes a broadcast operation, that add overhead depending on the number of cores involved. There are two broadcast implementations available. One adds a parallel overhead of \(0.0001n\), the other one \(0.0005 \log n\). For which number of cores do you get the highest speedup for both implementations?
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S_1(n) = \frac{1}{0.001 + \frac{1}{n}0.999 + 0.0001n}
\]

\[
S_2(n) = \frac{1}{0.001 + \frac{1}{n}0.999 + 0.0005\log(n)}
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$$S_2(n) = \frac{1}{0.001 + \frac{1}{n} 0.999 + 0.0005 \log(n)}$$

We can get the maximum of these terms if we minimize the term in denominator.

$$\frac{d}{dn} 0.001 + \frac{1}{n} 0.999 + 0.0001n = 0 \iff 0.0001 - \frac{0.999}{n^2} = 0 \iff n \approx 100$$

$$\frac{d}{dn} 0.001 + \frac{1}{n} 0.999 + 0.0005 \log(n) = 0 \iff \frac{0.005n \cdot 0.999}{n^2} = 0 \iff n = 1998$$
PRAM: Parallel Random Access Machine

- P processes with shared memory
- Ignores communications and synchronization
- Instruction are composed by 3 phases:
  - Load data from shared memory (if needed)
  - Perform computation (if any)
  - Store data in shared memory (if needed)
- Any process can read/write to any memory cell
  - How conflicts are handled?
PRAM: Conflicting Accesses

- **EREW: Exclusive Read / Exclusive Write**
  - No two processes are allowed to read or write to the same memory cell simultaneously

- **CREW: Concurrent Read / Exclusive Write**
  - Simultaneous reads are allowed; only one process can write

- **CRCW: Concurrent Read / Concurrent Write**
  - Simultaneous reads and write to the same memory cell are allowed
  - Priority CRCW: processors assigned fixed distinct priorities, highest priority wins
  - Random CRCW: one randomly chosen write wins
  - Common CRCW: all processors are allowed to complete write if and only if all the values to be written are equal

Weak: EREW < CREW < CRCW-C < CRCW-R < CRCW-P

Strong:
PRAM: Reduction

- Reduce p values on the p-processor EREW PRAM in $O(\log p)$ time
- The algorithm uses exclusive reads and writes
- It’s the basis of other EREW algorithms
PRAM: First 1

- Computing the position of the first one in the sequence of 0’s and 1’s in a constant time.

**Algorithm A**

(2 parallel steps and \(n^2\) processors)

- for each \(1 \leq i < j \leq n\) do in parallel
  - if \(C[i] = 1\) and \(C[j] = 1\) then \(C[j] := 0\)

- for each \(1 \leq i \leq n\) do in parallel
  - if \(C[i] = 1\) then \(\text{FIRST-ONE-POSITION} := i\)
PRAM: First 1 – Reducing Number of Processors

Algorithm B: it reports if there is any one in the table.

There-is-one:=0
for each 1 \leq i \leq n do in parallel
  if C[i] =1 then There-is-one:=1
PRAM: First 1 – Reducing Number of Processors

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Merge A and B

1. Partition table C into segments of size \( \sqrt{n} \)
2. In each segment apply the algorithm B
3. Find position of the first one in these sequence by applying algorithm A
4. Apply algorithm A to this single segment and compute the final value
PRAM: First 1 – Reducing Number of Processors

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Merge A and B
1. Partition table C into segments of size $\frac{n}{2}$.
2. In each segment apply the algorithm B
3. Find position of the first one in these sequence by applying algorithm A
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How many processors we need?

What’s the complexity?
PRAM: First 1 – Reducing Number of Processors

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How many processors we need?
(√n)² = n

What’s the complexity?
3 parallel steps → O(1)

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Exercise 3

How can we find the minimum from an unordered collection of $n$ natural numbers on EREW-PRAM machine?
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We can find the minimum from an unordered collection of $n$ natural numbers by performing a reduction along a binary tree: In each round, each processor compares two elements, and the smaller element gets to the next round, the bigger one is discarded. What is the work and depth of this algorithm?
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The dependency graph of this computation is a tree with $\log_2(n)$ levels. Therefore the longest path, which is equal to the depth/span has length $\log_2(n)$. The tree contains $2n - 1$ nodes, which is equal to the work.
Exercise 4

Develop an algorithm which can find the minimum in an unordered collection of \( n \) natural numbers in \( O(1) \) time on a CRCW-PRAM machine.
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Develop an algorithm which can find the minimum in an unordered collection of n natural numbers in $O(1)$ time on a CRCW-PRAM machine.

- Assume the list is stored in an array $A$.
- Create an additional array $tmp[n]$ initialized with $true$.
- We use $O(n^2)$ processors, labelled $p(i, j)$ with $0 \leq i, j \leq n$.
  - If true then $tmp[i]$ is set to false (it cannot be the minimum)
  - Otherwise nothing is done
- At the end we have only one element of $tmp$ set to true, say $tmp[k]$. The minimum element of $A$ is $A[k]$. 
Computation

- Usually, floating point performance (Gflop/s) is the metric of interest
- Road to peak in-core performance:

Instruction Level Parallelism (ILP)
Computation

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  - Improve ILP and apply SIMD
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• Road to peak in-core performance:
  ▪ Improve ILP and apply SIMD

Instruction Level Parallelism (ILP)

▪ Balance floating-point operation mix: equal number of additions and multiplications

  Hardware may have Fused Multiple-Add instructions (FMA) or equal number of adders/multipliers

Single Instruction Multiple Data (SIMD)
Communication

- DRAM bandwidth (GB/s) is the metric of interest

```
for (i=0; i<n; i++)
    for (j=0; j<n; j++)
        a[i][j] = a[i][j] + c[i][j] * d;

for (i=0; i<n; i++)
    for (j=0; j<n; j++)
        a[j][i] = a[j][i] + c[j][i] * d;
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  - Engages the hardware preficher

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• Use software prefetching
  ▪ Depending on the architecture, HW prefetcher can take time (e.g., 5 loads) to start prefetching
  ▪ SW prefetching can provide speedups for complex access patterns

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Locality

• 3Cs Model

  ▪ **Compulsory:** On the first access to a block; the block must be brought into the cache; also called cold start misses, or first reference misses.

  ▪ **Capacity:** Occur because blocks are being discarded from cache because cache cannot contain all blocks needed for program execution (program working set is much larger than cache capacity).

  ▪ **Conflict:** In the case of set associative or direct mapped block placement strategies, conflict misses occur when several blocks are mapped to the same set or block frame; also called collision misses or interference misses.

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Absolut Miss Rates on SPEC92

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What is the lower bound to the number of memory operations?

How to lower capacity misses?

How to lower conflict misses?

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What is the lower bound to the number of memory operations?

How to lower capacity misses?

How to lower conflict misses?

Can we lower compulsory misses?

Absolut Miss Rates on SPEC92

How to Improve Locality?

• Merging Arrays

    /* Before: 2 sequential arrays */
    int val[SIZE];
    int key[SIZE];

    /* After: 1 array of structures */
    struct merge {
        int val;
        int key;
    };
    struct merge merged_array[SIZE];

• Loop Interchange
• Loop Fusion
• Blocking or “tiling”
How to Improve Locality?

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• Reduce conflicts between key and val
• Improve spatial locality

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• Loop Fusion
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How to Improve Locality?

- Merging Arrays
- Loop Interchange

```c
/* Before */
for (k = 0; k < 100; k = k+1)
    for (j = 0; j < 100; j = j+1)
        for (i = 0; i < 5000; i = i+1)
            x[i][j] = 2 * x[i][j];

/* After */
for (k = 0; k < 100; k = k+1)
    for (i = 0; i < 5000; i = i+1)
        for (j = 0; j < 100; j = j+1)
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        for (j = 0; j < 100; j = j+1)
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```

Improves spatial locality: sequential access instead of striding through memory every 100 words

- Loop Fusion
- Blocking or “tiling”
How to Improve Locality?

• Merging Arrays
• Loop Interchange
• Loop Fusion

/* Before */
for (i = 0; i < N; i = i+1)
  for (j = 0; j < N; j = j+1)
    a[i][j] = 1/b[i][j] * c[i][j];
for (i = 0; i < N; i = i+1)
  for (j = 0; j < N; j = j+1)
    d[i][j] = a[i][j] + c[i][j];
/* After */
for (i = 0; i < N; i = i+1)
  for (j = 0; j < N; j = j+1)
    { a[i][j] = 1/b[i][j] * c[i][j];
      d[i][j] = a[i][j] + c[i][j];
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    }
```

- From two misses per access to a & c to one miss per access
- Improve temporal locality

- Blocking or “tiling”
How to Improve Locality?

• Merging Arrays
• Loop Interchange
• Loop Fusion
• Blocking or “tiling”
  ▪ Example: matrix multiplication
  ▪ Goal: reduce the working set
Compute/Memory Bound

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• What do we mean by “memory bound”?
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  ▪ It has high operations intensity
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• Roofline model helps to clarify  
  ▪ Plots the performance (GFlops/second) as a function of the Operational Intensity (GFlops/byte)  
  ▪ What’s Operational Intensity?
Operational Intensity

How many Flops per byte does your code show?

- **Work**: $W$ is the number of operations performed by a given program
- **Memory Traffic**: $Q$ is the number of bytes transferred from memory by a given program
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![Diagram of matrix multiplication](image)
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  ▪ **Example:** matrix multiplication (3 nested loops)
    \[
    W(n) = \sim n^3 \\
    Q(n) = n^2 \\
    \]

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    I(n) = \frac{W(n)}{Q(n)} = \sim n
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Roofline Model

Attainable GFlops/sec = Min(Peak Floating Point Performance, Peak Memory Bandwidth x Operational Intensity)

- A kernel with a given OI lies somewhere in the vertical line with x=OI
- Ridge point: intersection of the diagonal and horizontal roof
  - Its x-coordinate is the minimum operational intensity required to achieve maximum performance
  - It suggests the level of difficulty for programmers and compiler writers to achieve peak performance
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• Can issue 2 FP SSE2 instructions per cycle
• Slightly faster clock rate
• >4x gain in peak performance w.r.t. X2
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Ridge Point shifts right from 1.0 to 4.4
Adding Ceilings

• What if your program is far from the roofline?
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Cache usage optimizations can increase the OI, hence put a kernel in a different optimization region.

First improve OI, then apply other optimizations.
Models & Results
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(e) IBM Cell (QS20)

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GRFlop/s vs Operational Intensity (Flops/Byte)

- Peak DP + FMA
- Peak DP + SIMD
- Peak DP + ILP
- TLP only

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Legend:

- SpMV
- LBM-HD
- FFT (4K)
- FFT (512)
- without W/L NR
- without Memory Affinity
- peak stream bandwidth
- peak stream bandwidth
Models & Results
Multithreading

- The ridge point shifts from 1.3 to 4.6
- Increasing the input makes parallelization gain efficiency
  - Until when the working set gets too big to stay in cache

Applying the Roofline Model

• For each kernel, we need to measure:
  ▪ The work $W$
    
    Counters for floating point operations
  
  ▪ The runtime $T$
    
    Read Time Stamp Counter (RDTSC) is still a right choice
  
  ▪ The memory traffic $Q$
    
    LLC misses can be an underestimation
    
    Measure raw traffic on the memory controller if possible (i.e., Intel PCM)

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  ▪ The peak performance $\pi$: microbenchmarks or manual
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Applying the Roofline Model

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  - The work $W$
    - Counters for floating point operations
    $$W = \text{Scalar
double} + \text{SSE
double} \times 2 + \text{AVX
double} \times 4$$
    - E.g., $W$ on a Sandy Bridge platform
  - The runtime $T$
    - Read Time Stamp Counter (RDTSC) is still a right choice
  - The memory traffic $Q$
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LibLSB: https://spcl.inf.ethz.ch/Research/Performance/LibLSB/