

SlimSell: A Vectorizable Graph Representation for Breadth-First Search

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Abstract—Vectorization and GPUs will profoundly change graph processing. Traditional graph algorithms tuned for 32- or 64-bit based memory accesses will be inefficient on architectures with 512-bit wide (or larger) instruction units that are already present in the Intel Knights Landing (KNL) manycore CPU. Anticipating this shift, we propose SlimSell: a vectorizable graph representation to accelerate Breadth-First Search (BFS) based on sparse-matrix dense-vector (SpMV) products. SlimSell extends and combines the state-of-the-art SIMD-friendly Sell- $C\sigma$ matrix storage format with tropical, real, boolean, and sel-max semiring operations. The resulting design reduces the necessary storage (by up to 50%) and thus pressure on the memory subsystem. We augment SlimSell with the SlimWork and SlimChunk schemes that reduce the amount of work and improve load balance, further accelerating BFS. We evaluate all the schemes on Intel Haswell multicore CPUs, the state-of-the-art Intel Xeon Phi KNL manycore CPUs, and NVIDIA Tesla GPUs. Our experiments indicate which semiring offers highest speedups for BFS and illustrate that SlimSell accelerates a tuned Graph500 BFS code by up to 33%. This work shows that vectorization can secure high-performance in BFS based on SpMV products; the proposed principles and designs can be extended to other graph algorithms.

Code: <https://spcl.inf.ethz.ch/Research/Performance/SlimSell>

I. INTRODUCTION

Upcoming CPUs armed with wide vector instruction units as well as GPUs with even wider warps of cores will transform the way graph algorithms are reasoned about, developed, and executed. Graph schemes are traditionally optimized for architectures based on 32- or 64-bit instructions. This is not only due to the prevalence of such systems but also because graph processing is most often based on irregular fine-grained memory accesses [19]. With the trend to develop machines deploying large vector instruction or SIMD units, we must rethink the design of graph algorithms to use the available hardware effectively.

One such important algorithm is Breadth-First Search (BFS) [7] that is used in many scientific domains such as machine learning, data mining, and computational sciences. Moreover, it has applications in various graph-related problems, including bipartiteness testing and the Ford-Fulkerson method. Thus, despite the wealth of existing optimizations for BFS, the growing amounts and sizes of graph datasets require even faster BFS schemes.

It is well-known that BFS can be viewed in either the traditional combinatorial or the algebraic abstraction. *Traditional BFS* is based on primitives such as queues. *Algebraic BFS* is a series of matrix-vector (MV) products over various semirings [13]; the products consist of a sparse matrix and

a dense vector (SpMV) or a sparse matrix and a sparse vector (SpMSpV). BFS based on SpMV (BFS-SpMV) uses no explicit locking or atomics and has a succinct description as well as good locality [13]. Yet, it needs more work than traditional BFS and BFS based on SpMSpV [29].

There exist some BFS schemes for GPUs [25, 22, 6, 29, 9, 12]. However, they usually underutilize the available SIMD and vectorization parallelism as they focus on work-optimal traditional BFS or BFS based on SpMSpV that use fine-grained irregular memory accesses. Moreover, they are often tuned to a given architecture and thus not portable. In this work, we illustrate that even if BFS-SpMV is not work-optimal, one can use vectorization to outweigh potential performance penalties and secure high-performance. For this, we first show how to combine the Sell- $C\sigma$ [14] sparse matrix storage format with the algebraic BFS based on tropical, real, boolean, and sel-max semirings. Intuitively, Sell- $C\sigma$ decomposes a matrix into *chunks* stored in such a way that each chunk can be processed without additional overheads by the whole SIMD execution unit. We conduct a work/storage complexity and performance analysis and discover which semiring is the most advantageous for BFS-SpMV based on Sell- $C\sigma$ for a large selection of parameters. To the best of our knowledge, this is the first theoretical work complexity analysis as well as performance study on the benefits and downsides of each considered semiring.

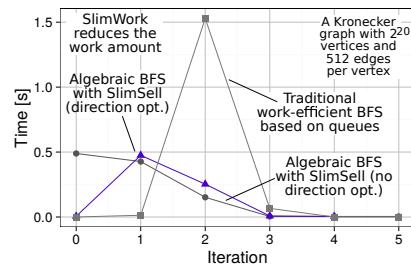


Figure 1: Time to compute each BFS iteration for a Kronecker power-law graph on an Intel Xeon Phi Knights Landing manycore CPU.

The advantage of Sell- $C\sigma$ is that it enables portable performance for SpMV products on CPUs and GPUs. Still, Sell- $C\sigma$ was not originally built for graph processing where it does not perform well. To alleviate this, we propose SlimSell: a vectorizable graph representation that needs up to 50% less storage than Sell- $C\sigma$, lowering the pressure on the memory subsystem when traversing undirected graphs. Intuitively, we do not explicitly store non-zero entries of the adjacency matrix but instead derive them implicitly from column indices. We then augment SlimSell with the SlimWork and the SlimChunk schemes to reduce the amount of work and load imbalance, and thus accelerate BFS even further.

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Here, two key ideas are to: skip chunks of computations if they correspond to final output values (e.g., vertex distances) that would not change, and divide large chunks among multiple compute units; an example illustration of SlimSell advantages is in Figure 1. We then analyze the work and storage complexity of BFS based on SlimSell and derive bounds for general graphs as well as for graph models that follow uniform (Erdős-Rényi) and power-law vertex degree distributions. Our evaluation on multi- and manycore CPUs and GPUs shows that the resulting BFS-SpMV outperforms traditional BFS by up to 33%. Finally, this is one of the first works to report BFS results on the state-of-the-art Intel Knights Landing (KNL) Xeon Phi manycore.

We provide the following contributions:

- We combine the state-of-the-art Sell- $C\text{-}\sigma$ matrix storage format with algebraic BFS based on tropical, boolean, real, and sel-max semirings. We conduct work/storage complexity and performance analysis and show which semiring secures the highest performance.
- We introduce SlimSell, a vectorizable graph representation that improves the storage complexity of Sell- $C\text{-}\sigma$ and accelerates BFS based on SpMV products.
- We propose SlimWork and SlimChunk, two schemes that reduce the amount of work and improve load balancing in BFS based on SlimSell.
- We evaluate SlimSell and show performance improvements of 33% over the optimized Graph500 BFS code and storage reductions of 50% over Sell- $C\text{-}\sigma$. Our work covers multi- and manycore CPUs as well as GPUs, with *the total of seven different systems*; we provide one of the first BFS results on the Intel KNL manycore.

II. BACKGROUND

We start with presenting the utilized concepts.

A. Notation

For convenience, Table I lists the most important symbols.

1) *Graph Structure*: We describe a graph G as a tuple (V, E) ; V is a set of vertices and $E \subseteq V \times V$ is a set of edges between vertices; $|V| = n$ and $|E| = m$. \mathbf{A} is the adjacency matrix of G . G 's diameter is denoted as D .

2) *Linear Algebra*: Bold symbols refer to vectors and matrices while standard font indicates a vector/matrix element. The matrix-vector (MV) multiplications are denoted with \otimes . The element-wise vector-vector (Hadamard) product is referred to with \odot . The lower index is used to indicate the iteration number (e.g., \mathbf{x}_k is \mathbf{x} in iteration k) while the upper index refers to a vector element (e.g., x_k^s is the s th element of \mathbf{x}_k); we also use square brackets when referring to vector elements in the source code when they are implemented with arrays ($x_k^s \equiv x_k[s]$). The *logical negation* of a vector \mathbf{x} is an element-wise operation $\bar{\mathbf{x}}$ where $\bar{x}^s = 0$ if $x^s \in \mathbb{R} \setminus \{0\}$, and $\bar{x}^s = 1$ if $x^s = 0$ (e.g., $(0, 7, 0)^T = (1, 0, 1)^T$).

B. Vectorization: Concepts and Considered Architectures

Modern x86 CPUs feature single instruction, multiple data (SIMD) execution units (also called *vector instruction units*) [18]. One unit has several *lanes* that proceed

Graph struct.	G n, m \bar{p}, D	A graph $G = (V, E)$; V and E are sets of vertices and edges. Numbers of vertices and edges in G ; $ V = n$, $ E = m$. Average degree and the diameter of G , respectively.
Algebraic notation	\otimes, \odot \mathbf{A}, \mathbf{A}' $\mathbf{x}_k, \mathbf{f}_k$ \mathbf{d}, \mathbf{p} $DP(\mathbf{d})$	Matrix-vector (MV); element-wise vector-vector (VV) product. G 's adjacency matrix and the transformed \mathbf{A} used in § III-A1. The result of $\mathbf{A} \otimes \mathbf{f}_k$; the frontier of vertices in iteration k . Distances (to the root) and parents (in the BFS traversal tree). A transformation that derives vertex parents \mathbf{p} from \mathbf{d} .
Various	T, W C, n_c σ	The number of threads; work complexity of a given scheme. Chunk height; the number of chunks in SlimSell or Sell- $C\text{-}\sigma$. Sorting scope in SlimSell and Sell- $C\text{-}\sigma$ ($\sigma \in [1, n]$).

Table I: The most important symbols used in the paper.

```

1 // Notes:  $\mathbf{V}$  is a vector of length  $C$  of int:  $\mathbf{V} \equiv \text{int}[C]$ .
2 // The names of the used Intel/NVIDIA functions can be found in
3 // the technical report1 due to space constraints.
4
5 V LOAD(V* addr); // Load and return  $C$  elements from addr.
6 void STORE(V* addr, V data); // Store data at address addr.
7 V [t1, t2, ..., t $\ell$ ]; // Create a vector of  $C$  elements.
8
9 // Compare a and b elementwise using operand op; return a vector
10 // with binary outcome of each comparison (0/1 if
11 // different/same); op can be EQ (equality), NEQ (non-equality).
12 V CMP(V a, V b, Op op);
13
14 // Interleave elements of a and b based on mask elements;
15 //  $\forall i \in [0, C] : \text{out}[i] = \text{mask}[i] ? b[i] : a[i]$ 
16 V BLEND(V a, V b, V mask);
17
18 // Return t elementwise result of the function FUN applied to
19 // a and b. FUN can be: MIN (minimum), MAX (maximum), ADD (sum),
20 // MUL (product), AND (logical and), OR (logical or).
21 V FUN(V a, V b);

```

Listing 1: Used vectorization functions: syntax and semantics.

synchronously in parallel and execute a specified scalar instruction on a data vector; each lane processes a vector element of a specified size. In modern CPUs with AVX (Advanced Vector Extensions), registers that hold the vectors are 256-bit wide, enabling 8 single-precision (or 4 double-precision) floating point operations per instruction. Consequently, the *SIMD width* is respectively 8 and 4. Next, manycores such as Xeon Phi KNL use wider SIMD units; KNL comes with 512-bit wide units. Finally, GPUs employ SIMT where *CUDA cores* roughly correspond to SIMD lanes. They are scheduled in *warps*; one warp usually counts 32 cores, which constitutes the GPU “SIMD width”. We present the used vectorization functions in Listing 1. For a widespread analysis of SlimSell, we evaluate all three types of architectures: Intel CPUs (represent classic latency-oriented x86 multicores), Intel Xeon Phi KNL (stands for state-of-the-art manycores), and NVIDIA GPUs (represent modern throughput-oriented SIMT GPUs).

C. Algorithms: BFS in Various Abstractions

The goal of BFS is to visit each vertex in G . First, it visits the neighbors of a specified *root* vertex r , then all the unvisited neighbors of r 's neighbors, and so on. Vertices that are processed in a current step constitute the BFS *frontier*. BFS outputs either the distance (in hops) from each vertex to r , or the parent of each vertex in the BFS traversal tree. Distances are stored in a vector $\mathbf{d} \in \mathbb{R}^n$ (d^v is the distance from vertex v to r) and parents in $\mathbf{p} \in \mathbb{R}^n$ (p^v is the parent of vertex v). \mathbf{d} can be transformed into \mathbf{p} using $O(m + n)$ work and $O(1)$ depth. To achieve this, for each vertex v , the neighbor w of v with the distance $d^w = d^v - 1$ must be

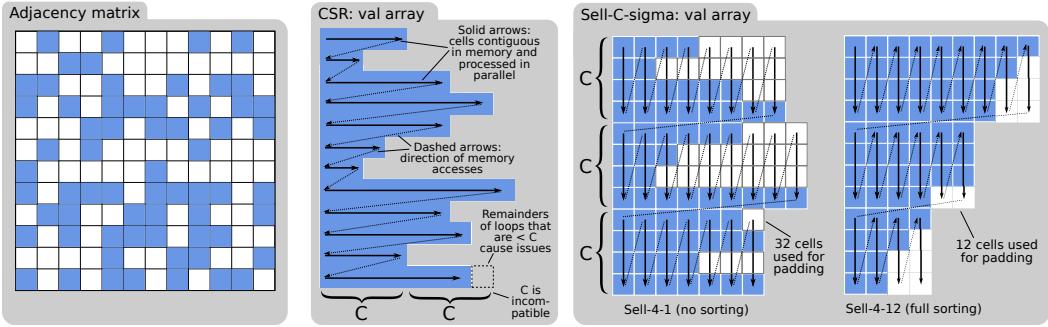


Figure 2: CSR and Sell- $C\text{-}\sigma$ constructed from an adjacency matrix. We only show *val* arrays that illustrate the differences between representations.

found; we refer to it as the *DP transformation* ($\mathbf{p} = DP(\mathbf{d})$).

1) *Traditional BFS*: Here, a frontier is implemented with a queue Q . At every iteration, vertices are removed in parallel from Q and all their unvisited neighbours are appended to Q ; this process is repeated until Q is empty.

2) *Algebraic BFS*: BFS can also be implemented with the MV product over a selected semiring. For example, for the real semiring, $\mathbf{x}_0 \in \mathbb{R}^n$ is a starting vector with $x_0^r = 1$ and 0 elsewhere. Then, for iteration $k \geq 1$, $\mathbf{x}_k = \mathbf{A} \otimes \mathbf{f}_{k-1}$ (we assume that \mathbf{A} is pre-transposed in accordance with common practice [5]); \mathbf{f}_{k-1} is the frontier in iteration $k-1$; note that $\mathbf{f}_0 = \mathbf{x}_0$. As we show in § III-A, for some semirings $\mathbf{f}_k = \mathbf{x}_k$, while for others one must derive \mathbf{f}_k from \mathbf{x}_k . \mathbf{x} and \mathbf{f} can be represented either as sparse or dense vectors that respectively result in sparse-sparse and sparse-dense $\mathbf{A} \otimes \mathbf{f}$ products; the latter entail more work but offer more potential for vectorization that we use in SlimSell.

D. Data Structures: CSR, Sell- $C\text{-}\sigma$, and Adjacency List

Finally, we discuss data structures relevant for our work.

1) *Compressed Sparse Row (CSR)*: In the well-known CSR format (see Figure 2), a matrix is represented with three arrays: *val*, *col*, and *row*. *val* contains all \mathbf{A} 's non-zeros (that correspond to G 's edges) in the row major order. *col* contains the column index for each corresponding value in *val* and thus has the same size ($O(m)$). Finally, *row* contains starting indices in *val* (and *col*) of the beginning of each row in \mathbf{A} (size $O(n)$). CSR is widely adopted for its simplicity and low memory footprint for sparse matrices. Yet, it hinders high-performance vectorization. Consider the CSR-based textbook MV product in Listing 2 where we unroll the inner loop. Such unrolling ensures consecutive data accesses necessary to effectively use vectorization (consecutive *val* entries are exposed). Yet, due to the reduction (line 8) and the cleanup of the loop remainder (line 10), the unrolling becomes inefficient for sparse matrices [14].

```
1 /* The code computes  $\mathbf{x}_{k+1} = \mathbf{A} \otimes \mathbf{x}_k$  using CSR. */
2 for(int i = 0; i < n; i++) {
3     int t_0 = t_1 = t_2 = t_3 = 0;
4     for(int j = row[i]; j < row[i+1]; j += 4) {
5         t_0 += val[j+0]*x_k[col[j+0]]; t_1 += val[j+1]*x_k[col[j+1]];
6         t_2 += val[j+2]*x_k[col[j+2]]; t_3 += val[j+3]*x_k[col[j+3]];
7     }
8     x_{k+1}[i] = t_0 + t_1 + t_2 + t_3; // Reduction.
9     // Clean up the loop remainder:
10    for(j=j-4; j < row[i+1]; j++) {x_{k+1}[i] += val[j]*x_k[col[j]]};}}
```

Listing 2: (§ II-D1) MV product with CSR and 4-way loop unrolling. Data alignment is assumed for clarity.

```
1 /* The code computes  $\mathbf{x}_{k+1} = \mathbf{A} \otimes \mathbf{x}_k$  using Sell- $C\text{-}\sigma$ . */
2 for(int i = 0; i < n/C; ++i) {
3     for(int j = 0; j < cl[i]; ++j) {
4         x_{k+1}[i*C+0] += val[cs[i]+j*C+0] * x_k[col[cs[i]+j*C+0]];
5         x_{k+1}[i*C+1] += val[cs[i]+j*C+1] * x_k[col[cs[i]+j*C+1]];
6         x_{k+1}[i*C+2] += val[cs[i]+j*C+2] * x_k[col[cs[i]+j*C+2]];
7         x_{k+1}[i*C+3] += val[cs[i]+j*C+3] * x_k[col[cs[i]+j*C+3]]; } }
```

Listing 3: (§ II-D2) The MV product kernel with Sell- $C\text{-}\sigma$ (C is 4).

2) *Sell- $C\text{-}\sigma$ Format*: To overcome the issues in CSR, Kreutzer et al. proposed a sparse matrix format called Sell- $C\text{-}\sigma$ that exposes data parallelism portably across architectures with different SIMD widths [14]. Intuitively, the key move from CSR is to “turn by 90°” the layout of *val* and *col* in memory so that *consecutive SIMD lanescores can process in parallel consecutive rows of \mathbf{A}* . We illustrate Sell- $C\text{-}\sigma$ in Figure 2 and Listing 3. It has four arrays: *val*, *col*, *cs*, and *cl*. Like in CSR, *val* and *col* host non-zeros in \mathbf{A} and the related column indices. The difference is that they consist of contiguous *chunks*; each chunk contains C matrix rows. Chunk elements are stored in the *column major* order; chunks are consecutive in memory. The *cs* and *cl* arrays provide starting offsets and lengths of each chunk. Rows are zero-padded up to the longest row in a chunk. Similar-sized rows are stored together by sorting them by the length, reducing the amount of required padding. Finally, $\sigma \in [1, n]$ controls the sorting scope; a larger σ entails more sorting. In this work, we show how to adapt Sell- $C\text{-}\sigma$ to BFS and to improve its design for more performance.

3) *Adjacency List (AL)*: Finally, AL is the well-known graph representation that uses $2m+n$ memory cells to store an undirected and unweighted graph; it consists of an array with IDs of neighbors of each vertex (size $2m$) and an offset array with the beginning of the neighbor data of each vertex (size n). AL is used together with traditional BFS. We show that SlimSell has comparable or smaller size than AL and secures more performance for various types of graphs.

III. ACCELERATING BFS BASED ON SPMV

We now proceed to describe how to amortize and outweigh the inherent additional work in BFS-SpMV using vectorization and SIMD parallelism. The first key idea is to combine Sell- $C\text{-}\sigma$ with semirings to portably accelerate BFS-SpMV (§ III-A). The second core idea is to develop SlimSell, a vectorizable graph representation that builds upon Sell- $C\text{-}\sigma$ by making it more storage-efficient (§ III-B). Finally, we propose SlimWork (§ III-C) and SlimChunk

(§ III-D), two schemes that reduce the work amount and improve load balancing in BFS-SpMV based on SlimSell.

A. Combining Sell- $C\text{-}\sigma$ with Semirings

We now provide the first systematic comparison of semirings for BFS-SpMV, and combine them with Sell- $C\text{-}\sigma$; see Listing 4 for a BFS iteration (frontier expansion) with the considered semirings. A reader who is not interested in the following theoretical details can proceed directly to § III-B. A semiring is defined as a tuple $S = (X, op_1, op_2, el_1, el_2)$ where X is a set equipped with two binary operations op_1, op_2 such that (X, op_1) is a commutative monoid with identity element el_1 and (X, op_2) is a monoid with identity element el_2 . We denote matrix-vector multiplication and Hadamard products on semiring S as \otimes_S and \odot_S .

1) *The Tropical Semiring* $T = (\mathbb{R} \cup \{\infty\}, \min, +, \infty, 0)$: To use BFS with this semiring, one must first transform \mathbf{A} to \mathbf{A}' where each off-diagonal zero entry is ∞ . Next, one sets $x_0^r = 0$ and $x_0^s = \infty$, for $s \neq r$ (the initial distance to r and any other vertex is respectively 0 and ∞). Then, $\mathbf{x}_k = \mathbf{f}_k = \mathbf{A}' \otimes_T \mathbf{f}_{k-1}$. This BFS computes distances *after the final iteration*: $\mathbf{d} = \mathbf{x}_D$ (D is the diameter) with predecessors $\mathbf{p} = DP(\mathbf{d})$ (see § II-C for a description of DP).

```

1 // val, col, cs, cl are data structures in Sell-C-σ (see § II-D2);
2
3 for(int i = 0; i < nc; i++) { // Iterate over every chunk.
4     int index = cs[i]; // Get offset to chunk i.
5     V x = LOAD(&f_{k-1}[i*C]); // Load chunk i from frontier f_{k-1}.
6     for(int j = 0; j < c[i]; j++) { // Iterate over each column.
7         V vals = LOAD(&val[index]); // Load A' values.
8         // Create the rhs vector consisting of C f_{k-1} entries.
9         V rhs = [f_{k-1}[col[index+3]], f_{k-1}[col[index+2]],
10            f_{k-1}[col[index+1]], f_{k-1}[col[index+0]]];
11
12    // Compute x_k (versions differ based on the used semiring):
13 #ifdef USE_TROPICAL_SEMIRING
14     x = MIN(ADD(rhs, vals), x); TROPICAL SEMIRING
15 #elif defined USE_BOOLEAN_SEMIRING
16     x = OR(AND(rhs, vals), x); BOOLEAN SEMIRING
17 #elif defined USE_SELMAX_SEMIRING
18     x = MAX(MUL(rhs, vals), x); SEL-MAX SEMIRING
19 #endif
20     index += C;
21 }
22 // Now, derive f_k (versions differ based on the used semiring):
23 #ifdef USE_TROPICAL_SEMIRING
24     STORE(&f_k[i*C], x); TROPICAL SEMIRING
25 #elif defined USE_BOOLEAN_SEMIRING
26     // First, derive f_k using filtering.
27     V g = LOAD(&g_{k-1}[i*C]); // Load the filter g_{k-1}.
28     x = CMP(AND(x, g), [0,0,...,0], NEQ); STORE(&x_k[i*C], x);
29
30     // Second, update distances d; depth is the iteration number.
31     V x_mask = x; x = MUL(x, [depth,...,depth]);
32     x = BLEND(LOAD(&d[i*C]), x, x_mask); STORE(&d[i*C], x);
33
34     // Third, update the filtering term.
35     g = AND(NOT(x_mask), g); STORE(&g_k[i*C], g);
36 #elif defined USE_SELMAX_SEMIRING:
37     // Update parents.
38     V pars = LOAD(&p_{k-1}[i*C]); // Load the required part of p_{k-1}
39     V pnz = CMP(pars, [0,0,...,0], NEQ);
40     pars = BLEND([0,0,...,0], pars, pnz); STORE(&p_k[i*C], pars);
41
42     // Set new x_k vector.
43     V tmpnz = CMP(x, [0,0,...,0], NEQ);
44     x = BLEND(x, &v[i*C], tmpnz); STORE(&x_k[i*C], x);
45 #endif

```

Listing 4: One iteration (frontier expansion) of BFS-SpMV; C is 4. We omit the real semiring as it is very similar to the boolean one.

2) *The Real Semiring* $R = (\mathbb{R}, +, \cdot, 0, 1)$: Here, $x_0^r = f_0^r = 1$ and any other element of \mathbf{x}_0 and \mathbf{f}_0 equals 0 (i.e., only r is in the initial frontier). Then, $\mathbf{x}_k = \mathbf{A} \otimes_R \mathbf{f}_{k-1}$ and $\mathbf{f}_k = \mathbf{x}_k \odot_R \mathbf{g}_k$ where \mathbf{g}_k is the *filtering term*: $\mathbf{g}_k = \sum_{l=0}^{k-1} \mathbf{f}_l$.

Finally, $\mathbf{d} = \sum_{l=1}^D l \mathbf{f}_l$ and $\mathbf{p} = DP(\mathbf{d})$. This semiring results in code snippets similar to the following boolean semiring and we omit it due to space constraints.

3) *The Boolean Semiring* $B = (\{0, 1\}, |, \&, 0, 1)$: Similarly to the real semiring, $x_0^r = f_0^r = 1$ and $x_0^s = f_0^s = 0, s \neq r$. Next, $\mathbf{x}_k = \mathbf{A} \otimes_B \mathbf{f}_{k-1}$, and $\mathbf{f}_k = \mathbf{x}_k - \mathbf{g}_k$; $\mathbf{g}_k = \bigcup_{l=0}^{k-1} \mathbf{f}_l$, $k \geq 2$. Then, $\mathbf{d} = \bigcup_{l=1}^D l \mathbf{f}_l$ and $\mathbf{p} = DP(\mathbf{d})$.

4) *The Sel-Max (S) Semiring* $(\mathbb{R}, \max, \cdot, -\infty, 1)$: All the above BFS variants require the DP transformation to derive \mathbf{p} . We now present a semiring that facilitates computing parents. In this semiring $x_0^r = r$ and $x_0^s = 0, s \neq r$. The frontier is given by $f_0^r = 1$ and $f_0^s = 0, s \neq r$. Here, we also use an additional vector $\mathbf{p}_0 = \mathbf{x}_0$. Then, in each iteration, we first calculate $\mathbf{x}_k = \mathbf{A} \otimes \mathbf{x}_{k-1}$ and derive the current frontier $\mathbf{f}_k = \bar{\mathbf{x}}_k - \mathbf{g}_k$ where $\mathbf{g}_k = \sum_{l=0}^{k-1} \mathbf{f}_l$ ($\bar{\mathbf{x}}$ is a double logical negation to transform each non-zero in \mathbf{x} into 1). We next obtain $\mathbf{p}_k = \mathbf{p}_{k-1} + \bar{\mathbf{p}}_{k-1} \odot \mathbf{x}_k$. Moreover, \mathbf{x}_k must be updated in such a way that each non-zero element becomes equal to its index: $\mathbf{x}_k = \bar{\mathbf{x}}_k \odot (1, 2, \dots n)^T$. After the last iteration, we have $\mathbf{p} = \mathbf{p}_D$. Finally, $\mathbf{d} = \bigcup_{l=1}^D l \mathbf{f}_l$.

Work Complexity We compare work complexity W of BFS-SpMV based on Sell- $C\text{-}\sigma$ with other schemes in Table II. Full sorting that takes $O(n \log n)$ is assumed ($\sigma = n$). Still, we exclude this term as it is a one-time investment and it does not change the asymptotic complexity. Given vertices sorted in increasing order by degree, we let ρ_i denote the degree of the i th vertex and $\hat{\rho}$ denote the maximum vertex degree. Our results focus on the tropical semiring, results for other semirings follow similarly. We derive a general bound for W based only on C and the maximum degree $\hat{\rho}$ for any graph. We then apply this bound to obtain expected storage bounds for Erdős-Rényi and power-law graph models.

BFS algorithm	$ W $
Traditional BFS (textbook [7])	$O(n + m)$
Traditional BFS (bag-based [15])	$O(n + m)$
Traditional BFS (direction-inversion [12])	$O(Dn + Dm)$
BFS-SpMV (textbook [7])	$O(Dn^2)$
BFS-SpMV [9]	$O(Dn + Dm)$
BFS (SpMSpV with merge sort [29])	$O(n + m \log m)$
BFS (SpMSpV with radix sort [29])	$O(n + xm)$
BFS (SpMSpV with no sort [29])	$O(n + m)$
This work (graphs with max degree $\hat{\rho}$)	$O(Dn + Dm + DC\hat{\rho})$
This work (Erdős-Rényi graphs)	See Equation (1)
This work (power-law graphs)	See Equation (2)

Table II: Comparison of W ; x is the length of the largest key in binary [29].

The size of all the blocks (except the largest) is in total

$$\sum_{i=2}^{n_c} C \rho_{iC-1} \leq \sum_{i=1}^{n_c-1} \sum_{j=1}^C \rho_{(i-1)C+j} \leq m,$$

as the size of each block is smaller than the number of vertices in the previous (larger) block. Next, the size of the largest block is $\hat{\rho}C$, so the total storage is bounded by

$$\sum_{i=1}^{n_c} C \rho_{iC-1} \leq m + \hat{\rho}C.$$

This bound is illustrated in Figure 3. Asymptotically, this bound is always tight for Sell- $C\text{-}\sigma$, since the minimum

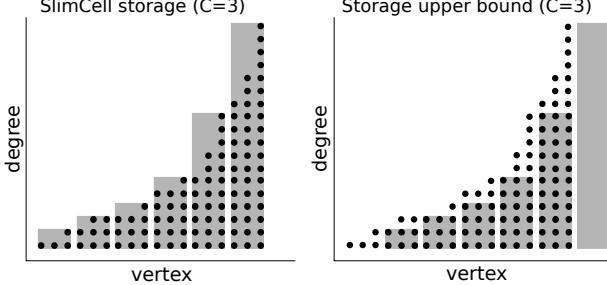


Figure 3: Justification of the upper bound on work and storage in Sell- $C\text{-}\sigma$ (for $C = 3$). Overall, the padding can generate at most $C\hat{\rho}$ extra storage where $\hat{\rho}$ is the maximum degree.

storage (a lower bound) is $\max(m, \hat{\rho}C)$.

To obtain a bound on W , we assume all vertices and edges need to be accessed at each of D steps, which yields

$$W = O(Dn + Dm + D\hat{\rho}C).$$

In Erdős-Rényi graphs, an edge exists with a probability p . A balls-into-bins argument [26] may be applied to bound the maximum vertex degree, (each bin can be thought of as a vertex in the adjacency matrix and each ball an outgoing edge). When $np = \Omega(\log(n))$, this analysis implies that the maximum degree of such a graph will be $\hat{\rho} = O(np)$. When p is very small, the same type of argument leads to a bound of $\hat{\rho} = O(\log(n))$. Therefore, we ascertain

$$W = O(Dn + Dm + DC \log(n)) \quad (1)$$

In power-law graphs, the probability that a vertex has degree ρ is $f(\rho) = \alpha\rho^{-\beta}$. To get a high-probability bound on the max degree of a power-law graph $\hat{\rho}$, we consider the probability that a vertex has degree $\rho \geq \hat{\rho}$,

$$P[\rho > \hat{\rho}] = \alpha \sum_{x=\hat{\rho}+1}^{n-1} x^{-\beta} \approx \alpha \int_{\hat{\rho}}^{\infty} x^{-\beta} dx = \alpha \frac{\hat{\rho}^{1-\beta}}{\beta - 1}.$$

To ensure that with probability $1 - 1/\log(n)$ all vertices have degree less than $\hat{\rho}$, we need

$$(1 - P[\rho > \hat{\rho}])^n \leq 1 - \frac{1}{\log(n)}.$$

This allows us to bound the maximum vertex degree with high probability (using Bernoulli's inequality),

$$\begin{aligned} P[\rho > \hat{\rho}] &\geq 1 - \left(1 - \frac{1}{\log(n)}\right)^{1/n} \\ \hat{\rho} &\geq \left(\frac{\beta-1}{\alpha} \left[1 - \left(1 - \frac{1}{\log(n)}\right)^{1/n}\right]\right)^{\frac{1}{1-\beta}} \\ &\geq \left(\frac{\beta-1}{\alpha} \frac{1}{n \log(n)}\right)^{\frac{1}{1-\beta}} = O\left((\alpha n \log(n))^{\frac{1}{\beta-1}}\right). \end{aligned}$$

Given this probabilistic bound on the maximum degree, we obtain a bound on the amount of work for power-law graphs,

$$W = O\left(Dn + Dm + DC(\alpha n \log(n))^{\frac{1}{\beta-1}}\right). \quad (2)$$

The analysis for other semirings differs in that more instructions are required to derive \mathbf{f} from \mathbf{x} in each iteration. These instructions take $O(n)$ of the total additional work to each term from the analysis for the tropical semiring.

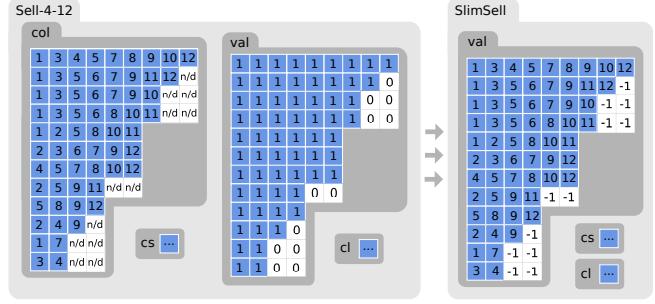


Figure 4: SlimSell: val can be inferred from col. $C = 4$, $\sigma = 12$.

B. Reducing Storage Complexity with SlimSell

We now build on Sell- $C\text{-}\sigma$ and introduce *SlimSell*: a representation for unweighted graphs that reduces the original Sell- $C\text{-}\sigma$ size by a factor of up to $\frac{m+n}{2m+n}$, putting less pressure on the memory subsystem. Our key notion is that, for undirected graphs, entries in \mathbf{A} only indicate presence or absence of edges; this information can be contained in *col* without any need for *val*. For this, each entry in *col* in SlimSell contains either a usual column index of the corresponding non-zero entry in \mathbf{A} (as in Sell- $C\text{-}\sigma$) or a special marker (e.g., -1) if the entry is not an edge but is only present due to padding. Thus, an entry in *col* different from the marker indicates an edge and implies a 1 in *val*. We illustrate SlimSell in Figure 4 and in Listing 5. Instead of directly loading *val* (like in Listing 4, line 7), we first load the corresponding column indices from *col* (Listing 5, line 8). Then, a vectorized compare instruction provides us with a mask that determines which column indices are -1 and which are non-negative entries corresponding to edges. Finally, we derive the contents of *val* (lines 10-12).

```

1 // Vectors used by SlimSell:
2 V m_ones = [-1, ..., -1], ones = [1, ..., 1], infns = [∞, ..., ∞];
3
4 for(int i = 0; i < n/C; i++) { // Iterate over each chunk.
5     int index = cs[i]; // get offset to chunk i.
6     V tmp = LOAD(&f_{k-1}[i*C]);
7     for(int j = 0; j < cl[i]; j++) { // Iterate over each column.
8         V cols = LOAD(&col[index]);
9         // Compute a mask that indicates which entry in cols is -1.
10        V vals = CMP(cols, m_ones, EQ);
11        // Derive required entries from val.
12        vals = BLEND(ones, infns, vals);
13        // Create the rhs vector consisting of four f_{k-1} entries.
14        V rhs = [f_{k-1}[col[index+3]], f_{k-1}[col[index+2]],
15                  f_{k-1}[col[index+1]], f_{k-1}[col[index+0]]];
16        tmp = MIN(ADD(rhs, vals), tmp); // Compute a new frontier.
17        index += C;
18    }
19    STORE(&f_k[i*C], tmp); } // Set a new frontier.

```

Listing 5: (§ III-B) An example of using SlimSell; C is 4.

SlimSell reduces data transfer by removing loads of *val*. Yet, more computation is required (lines 10-12). We show in § IV-A3 that this does not entail significant overheads and SlimSell offers more performance than Sell- $C\text{-}\sigma$.

Storage Complexity SlimSell reduces the size of not only Sell- $C\text{-}\sigma$ but also CSR and AL; see Table III for a summary. Sell- $C\text{-}\sigma$ and SlimSell require respectively $4m + \frac{2n}{C} + P$ and $2m + \frac{2n}{C} + P$ words; P is the number of cells from padding and it depends on a specific graph and its degree distribution. SlimSell uses less storage than the corresponding AL if:

$$2m + \frac{2n}{C} + P < n + 2m \Leftrightarrow P < n \left(1 - \frac{2}{C}\right) \quad (3)$$

This translates to $P < \frac{3n}{4}$ for $C = 8$ (e.g., in Xeon CPUs), $P < \frac{7n}{8}$ for $C = 16$ (e.g., in KNLs), and $P < \frac{7n}{8}$ for $C = 32$ (e.g., in Tesla GPUs). We show in an empirical analysis that covers various families of graphs (§ IV-E) that the impact of P is negligible for larger sorting scopes ($\sigma > \sqrt{n}$) and SlimSell always uses less space than CSR and Sell- $C\text{-}\sigma$ and it is comparable or more space-efficient than AL. Finally, note that the size of val in SlimSell and Sell- $C\text{-}\sigma$ ($= 2m + P$) is equal to the amount of work W of a single SpMV product. Thus, bounds (1) and (2) equal storage complexities for Erdős-Rényi and power-law graph models.

Representation	Sell- $C\text{-}\sigma$	CSR	AL	SlimSell
Size [cells]	$ 4m + \frac{2n}{C} + P $	$ 4m + n $	$ 2m + n $	$ 2m + \frac{2n}{C} + P $

Table III: (§ III-B) Storage complexity of considered graph representations; P is the number of padded memory cells.

```

1 // Frontier expansion: we start like in Listing 5.
2 for(int i = 0; i < n/C; i++) {
3     int skip = 1; // Assume we skip the current chunk
4     for(int j = 0; j < C; j++) {
5 #ifdef USE_TROPICAL_SEMIRING
6     if(fk_{-1}[i*C+j] == ∞) TROPICAL SEMIRING
7     skip = 0; // If any distance is still ∞, go on.
8 #elif defined USE_BOOLEAN_SEMIRING || BOOLEAN & REAL SEMIRING
9     defined USE_REAL_SEMIRING
10    if(gk_{-1}[i*C+j] != 0)
11    skip = 0; // If any filter is still ≠ 0, go on.
12 #elif defined USE_SELMAX_SEMIRING SEL-MAX SEMIRING
13    if(pk_{-1}[i*C+j] != 0)
14    skip = 0; // If any parent is still ≠ 0, go on.
15 #endif
16
17    if(skip) // Swap the frontiers.
18        store(&xk[i*C], load(&xk_{-1}[i*C])); continue;
19 /* Now, continue with the MV product as in Listing 4... */ }
```

Listing 6: (§ III-C1) SlimWork for various semirings; C is 4.

C. Reducing Work Amount with SlimWork

SlimSell improves upon Sell- $C\text{-}\sigma$ by reducing its size. We now introduce SlimWork (see Listing 6), a scheme that reduces the work amount in BFS-SpMV. Intuitively, we skip chunks of computation if they are associated with the final BFS values (distances or parent IDs) that do not change in future iterations. As our performance study shows (§ IV), this scheme significantly accelerates BFS-SpMV. We now present how to use SlimWork with each semiring.

1) *Tropical Semiring*: SlimWork for the tropical semiring is illustrated in Listing 6 (lines 5-7). Consider $f_k = A' \otimes f_{k-1}$. In the label-setting BFS, f_k^s can only differ from f_{k-1}^s if f_{k-1}^s is not the final distance. By verifying whether $f_k^s = f_{k-1}^s$, we determine if f_{k+1}^s has to be computed or whether it can simply be carried over from f_k (line 18).

2) *Other Semirings*: Real or boolean semirings require a vector for the filtering term $g_k = \sum_{l=0}^{k-1} f_l$ (see § III-A2) to verify if a given chunk of f_k must be updated. The computation in a chunk is skipped if all the rows in that chunk satisfy the condition that the corresponding entries of g_k are 0. A similar criterion (based on the p_k vector) is used for the selmax semiring; see Listing 6.

Work Complexity SlimWork adds $O(C)$ work per chunk as it must decide whether to omit chunks of computation. However, in return it may reduce W by $O(\hat{\rho}_i C)$ for each skipped chunk i ; $\hat{\rho}_i$ is the maximum degree in chunk i .

D. Improving Load Balance with SlimChunk

The final SlimChunk scheme aims at accelerating BFS-SpMV when executing on units with large SIMD widths. Specifically, consider a case with a large sorting scope (e.g., $\sigma = \sqrt{n}$). The rows are sorted by the degree of the corresponding vertices. Thus, some chunks (related to high-degree vertices) may entail much more computation than the chunks related to low-degree vertices, resulting in load imbalance. To alleviate this, we split A not only horizontally into chunks, but we also split the chunks vertically, in two dimensions. This still leads to the contiguous layout in memory but also accelerates BFS-SpMV by dividing work more equally between threads, as we show in § IV.

To conclude, SlimSell improves the design of BFS-SpMV along *three dimensions*: it reduces the size, lowers the amount of work, and improves the load balancing.

IV. PERFORMANCE ANALYSIS AND EVALUATION

We now illustrate that SlimSell secures high performance for BFS-SpMV. We also analyze the differences between BFS-SpMV based on various semirings and representations.

Selection of Benchmarks and Parameters We consider all four BFS-SpMV semiring variants. Next, performance and storage improvements from SlimSell, SlimWork, and SlimChunk are evaluated. Both strong- and weak-scaling is considered. We also analyze the *DP* transformation overheads (DP, No-DP). To evaluate the impact from sorting, we vary $\sigma \in [1, n]$ (for simplicity σ is a multiple of C). We verify the BFS performance in each iteration for a fine-grained analysis. Next, static and dynamic OpenMP scheduling is incorporated (omp-s, omp-d). Three classes of graphs are considered: synthetic power-law Kronecker [16] and Erdős-Rényi (ER) [10] graphs such that $n \in \{2^{20}, \dots, 2^{28}\}$ and $\bar{\rho} \in \{2^1, \dots, 2^{10}\}$; we also use real-world graphs (RW); see Table IV. Due to a very large amount of data we present and discuss in detail a small subset; the remainder can be found in the technical report (see the link on page 2).

Type	ID	n	m	$\bar{\rho}$	D
Kronecker graphs	K	1M-268M	2M-536M	2-1014	19-33
Social networks	orc	3.07M	117M	39	9
	pok	1.63M	30.6M	18.75	11
	epi	75k	508k	6.7	15
Ground-truth [30] community	ljn	3.99M	34.6M	8.67	17
Web graphs	brk	685k	7.60M	11.09	514
	gog	875k	5.1M	5.82	21
	sta	281k	2.31M	8.2	46
	ndm	325k	1.49M	4.59	674
Purchase network	amz	262k	1.23M	4.71	32
Road network	rca	1.96M	2.76M	1.4	849

Table IV: The analyzed graphs with skewed degree distributions.

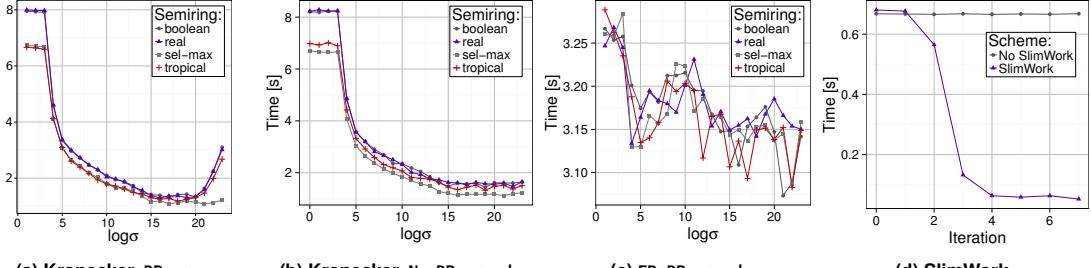


Figure 5: (§ IV-A) CPU analysis (Dora). The Kronecker graphs have $n = 2^{23}$, $\bar{\rho} = 16$; the ER graphs have $n = 2^{23}$, $p = 2 \cdot 10^{-6}$, $\bar{\rho} \approx 16$.

Comparison Targets (Performance) We compare BFS-SpMV equipped with SlimSell to the work-efficient highly-optimized OpenMP BFS Graph500 code [24] (Trad-BFS). This baseline applies several optimizations; among others it reduces the amount of fine-grained synchronization by checking if the vertex was visited before executing an atomic. As Trad-BFS is work-optimal, it also represents the work-optimal BFS based on SpMSpV. We execute Trad-BFS on both KNLs and CPUs to secure fair comparison and to illustrate *one of the points of our work: vectorization- and SIMD-friendly SlimSell enables BFS-SpMV to be comparable to work-efficient BFS optimized for CPUs.*

Comparison Targets (Storage) In the storage analysis, we compare SlimSell to CSR, AL, and Sell- $C\text{-}\sigma$.

Experimental Setup and Architectures We conduct the analysis on several CPUs, GPUs, and manycores, with the *total of seven evaluated systems*:

Dora (CPU) One node of the CSCS Piz Dora supercomputer contains two Intel Xeons E5-2695 v4 @ 2.10 GHz. Each CPU has 18 cores, 18x 256 KB L2 and 45 MB L3 cache. Each nodes has 64 GB of RAM. We use gcc-5.3.

Tesla (GPU) We use NVIDIA Tesla K80 GPUs from the CSCS Greina HPC cluster (covering high-performance GPUs). Any CPU code is compiled using gcc-5.3, the CUDA code uses cudatoolkit-6.5.

KNL (manycore) We use Intel Xeon Phi KNLs 7210 (also from Greina). Each KNL has 64 4-way 1.3GHz multi-threaded cores with the total of 32 MB L2 and 66 GB of RAM. We use icc 16.0.1.150.

Others Other systems are described in detail in the technical report. They include a Tesla K20X from the CSCS Piz Daint supercomputer, a Trivium server with an Intel Haswell CPU and an NVIDIA GTX 670 that represent commodity machines, and a Xeon E5-1620 @3.50GHz from CSCS Greina to cover very low-latency systems.

A. CPU Analysis (Xeon E5-2695 v4)

We start with the CPU analysis; see Figure 5. We fix C to match architectural constraints. For example, choosing 32-bit integers to represent vertex identifiers on a CPU yields a SIMD width of 8 due to 256-bit wide AVX registers. We use OpenMP for intra-node parallelization.

1) Impact from Sorting (σ): We first investigate the impact of σ for various BFS-SpMV scenarios (Figures 5a-5c). Performance strongly depends on σ as significantly

different vertex degrees in one C entail wasted work due to padding. Thus, large σ is preferable. Next, $\sigma < C$ does not reduce padding and work but only reorders rows within a chunk. Thus, the performance does not increase while $\log \sigma \leq 3$. Moreover, in Figure 5a, an overhead due to the DP transformation is visible as σ goes towards n , except for the sel-max semiring. This is because in static OpenMP scheduling all threads process similar counts of chunks. Then, for a very large σ , the first chunk contains all of the longest rows and consequently the corresponding thread performs the majority of work, causing imbalance. Dynamic OpenMP scheduling adds $\approx 1\text{-}2\%$ of relative overhead but alleviates the problem; see Figure 5b.

2) Differences between Semirings: The inner-most loop that processes chunks is the same for each semiring except for the used vector instructions (cf. Listing 4, lines 6-21). As Figure 5 shows, performance differences are negligible ($\approx 1\text{-}2\%$), confirming the intuition that BFS is memory-bound. However, semirings also differ in the post-processing that derives f_k from x_k (lines 22-45). The tropical semiring contains no additional work. Contrarily, the real and boolean semirings update the filter g_k (six instructions and two stores) while the sel-max semiring processes the p vector (four instructions and two stores). Still, the only major performance difference comes with the DP in sel-max semiring.

3) Advantages of SlimSell: We next illustrate advantages of SlimSell over Sell- $C\text{-}\sigma$ (Table V). Here, σ determines how much bandwidth is wasted on unused loads. Larger σ results in lower impact from SlimSell as the bandwidth is used more efficiently due to sorting.

σ	Boolean	Real	Tropical	Sel-max
2^4	1.17	1.17	1.21	1.18
2^{18}	1.00	1.04	1.04	1.03

Table V: Speedup of SlimSell over Sell- $C\text{-}\sigma$ in Kronecker graphs ($n = 2^{24}$, $\bar{\rho} = 16$).

4) Advantages of SlimWork: We present SlimWork advantages in Figure 5d. We compare BFS-SpMV variants with and without SlimWork for several σ s (for clarity, we plot only the case with $\sigma = n$). The larger σ , the faster work amount decreases with iterations. This is because larger σ s make it more probable that the majority of the largest chunks (associated with high-degree vertices) are processed in early iterations. Next, SlimWork skips chunks as soon as all the associated vertices have been visited. Thus, as more vertices are visited, the number of chunks left to compute

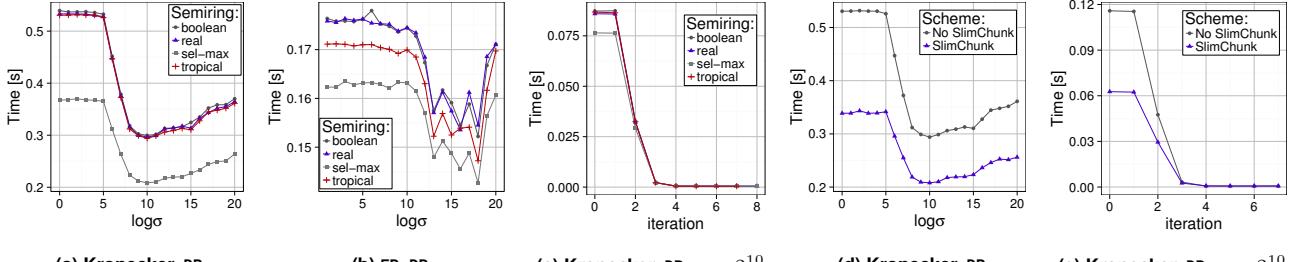


Figure 6: (§ IV-B) GPU analysis (Tesla K80). The Kronecker graphs have $n = 2^{20}$, $\bar{\rho} = 16$; the ER graphs have $n = 2^{18}$, $p = 1.5 \cdot 5 \cdot 10^{-5}$, $\bar{\rho} \approx 16$.

decreases and the last few iterations entail only little work. Contrarily, early iterations gain no speedup; they instead pay a small overhead for checking the skipping criteria. Still, the overhead is rapidly outweighed by saving expensive chunk computations. Overall, SlimWork accelerates the baseline SlimSell by a large factor, for example $\approx 129\%$ for sel-max for a Kronecker graph with $n = 2^{24}$, $\bar{\rho} = 16$. Finally, in “No SlimWork” (corresponding to Sell- C - σ augmented only with the SlimSell storage reductions), there is no performance improvement after the first iteration.

5) *Various Graph Families*: We now discuss Erdős-Rényi and real-world inputs. The degrees of the former follow the uniform instead of the power law distribution. The impact from large σ is therefore less evident; see Figure 5c. The fine-grained analysis of each BFS step illustrates that the decrease in time only starts during the final iterations. Next, we consider real-world graphs. Some, like amz or rca, have high D and low $\bar{\rho}$ (3.4 for amz and 1.4 for rca). This leads to small or no improvement from SlimWork, regardless of σ . Others behave similarly to Kronecker graphs as their $\bar{\rho}$ is large enough for SlimWork to ensure speedups.

B. GPU Analysis (Tesla K80)

We present a representative subset of results in Figure 6. Our insights are similar to those of the CPU analysis. The main difference is that wider SIMD units in GPUs secure higher speedups. First, Figures 6a and 6b depict the total execution time for varying σ for Kronecker and ER graphs. Similarly to CPUs, the performance does not improve up to a certain σ equal to C . Second, sel-max performs better than others as it does not need DP. Moreover, the performance for higher σ is because the sorting of the rows in \mathbf{A} leads to large load imbalance (e.g., see Figure 6b). Then, the per iteration performance follows patterns similar to CPUs as illustrated in Figure 6c. Finally, we show that SlimChunk brings expected significant advantages, for example $\approx 50\%$ in the first two iterations in Figure 6e).

C. Manycore Analysis (KNL)

Here, we evaluate SlimSell on Intel KNLs; see Figure 8. The latency of each iteration grows as expected with the increasing $\bar{\rho}$ or n . KNL secures a drop in compute time after the first iteration. In GPUs, this effect is less visible due to larger SIMD widths that hinder reducing computation. On CPUs, it is only negligibly visible in Figure 4d as Erdős-Rényi graphs are used there. Later (§ IV-F) we show that

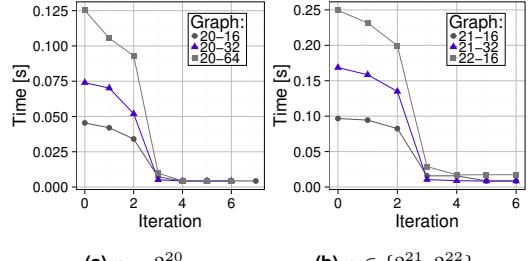


Figure 8: (§ IV-C, KNL analysis) A fine-grained analysis (using the tropical semiring) on Kronecker graphs; two numbers for each graph are $\log n \bar{\rho}$.

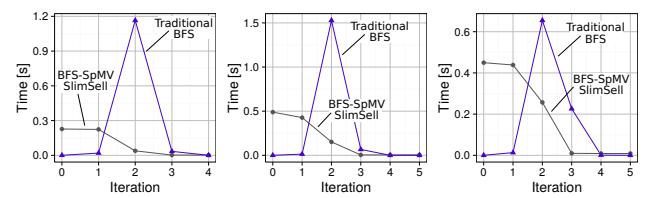


Figure 9: (§ IV-C, KNL analysis) Fine-grained comparison between BFS-Trad and BFS-SpMV with SlimSell and sel-max; C is 16, G is Kronecker. our variant of BFS-SpMV based on SlimSell outperforms the traditional work-efficient BFS on KNLs.

D. Preprocessing Analysis

We illustrate that the full sorting time required for good storage improvements as well as the actual build time can be amortized away. For a Kronecker graph with $n = 2^{24}$, sorting takes ≈ 0.95 s, which constitutes $\approx 21\%$ of a single BFS run. Thus, 10 BFS runs are enough to reduce the sorting time to $< 2\%$ of the total runtime. The build time is analogous to that of Sell- C - σ [14]; it lasts longer but can also be amortized with more BFS runs. For example, on a Kronecker graph with $n = 2^{18}$, 20 BFS runs are enough to reduce the full preprocessing time to $< 5\%$ of the total runtime. The results for other graphs are similar. In our analyses, we amortize the preprocessing time and report averaged iteration or total execution times.

E. Storage Analysis

Figure 7 illustrates storage improvements of SlimSell for various σ , n , $\bar{\rho}$, and graph families. SlimSell reduces the size of Sell- C - σ by $\approx 50\%$, a consistent advantage for various n , $\bar{\rho}$, and σ . Notably, for full sorting ($\sigma = n$) and for Kronecker graphs, SlimSell is also more compact than AL (by $\approx 5\text{-}10\%$) which is effectively the smallest graph representation if no compression is used. The same effect sets in for $\sigma \geq \sqrt{n}$ for

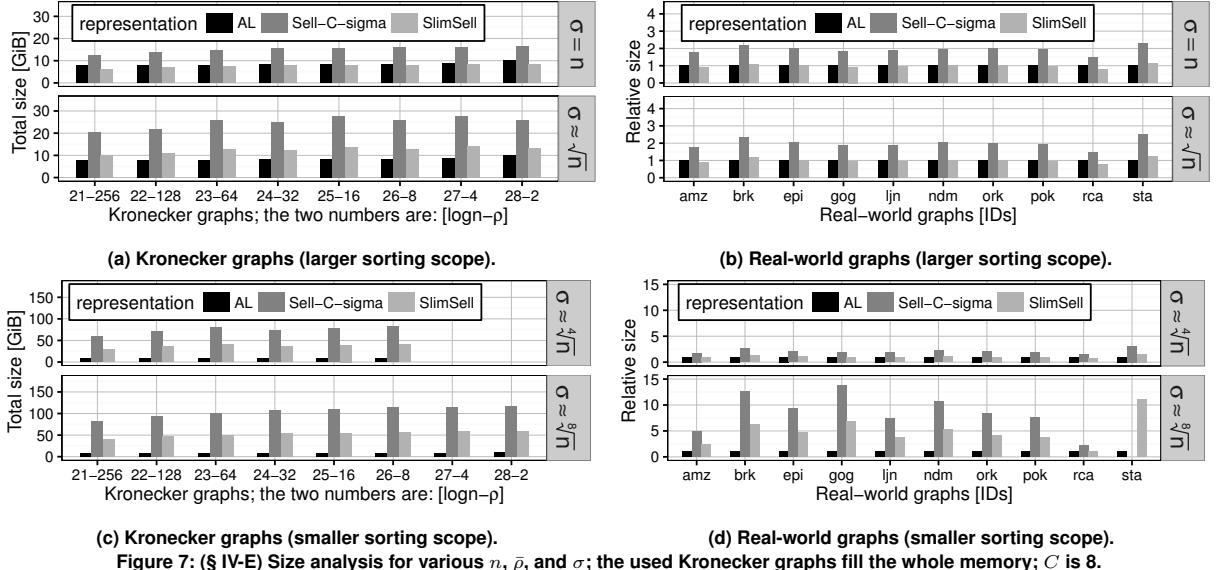


Figure 7: (§ IV-E) Size analysis for various n , $\bar{\rho}$, and σ ; the used Kronecker graphs fill the whole memory; C is 8.

RW graphs. Note that $C = 8$ in the above analysis. Larger C brings even more storage reductions.

F. Comparison to the State-of-the-Art

We compare BFS-SpMV equipped with SlimSell to Trad-BFS in a fine-grained analysis. Figure 10 shows the time to finish each BFS iteration for various $\bar{\rho} \in \{1, \dots, 512\}$; we compare the optimized traditional BFS running on a system where it achieves highest performance (Xeon CPU) with BFS-SpMV based on SlimSell that executes on Tesla K80 GPU. The higher $\bar{\rho}$ (denser G), the faster BFS-SpMV is. This is supported with the intuition: more edges in G entail a larger SIMD potential. Finally, Figures 1 and 9 show that BFS-SpMV based on SlimSell outperforms the traditional BFS by up to 53%; denser graphs entail larger speedups. As expected, power-law graphs are more SIMD-friendly during the expansion of the large frontier part. Contrarily, Erdős-Rényi graphs do not have this property. We conclude that SlimSell enables BFS-SpMV (running on throughput-oriented architectures such as GPUs) to match the performance of highly-optimized work-efficient codes (executing on optimized and latency-oriented CPUs).

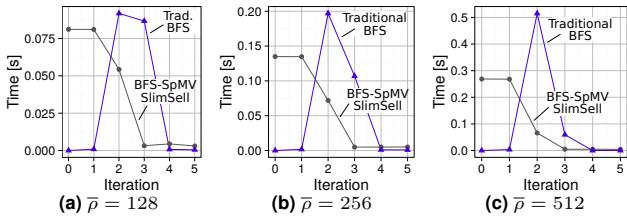


Figure 10: (§ IV-F) Fine-grained comparison between BFS-Trad (optimized for CPUs) and BFS-SpMV executing on GPUs based on the tropical semiring; C is 32, G is Kronecker, $n = 2^{20}$.

V. RELATED WORK

Extensive research has been done to address the challenges in parallel graph processing [19]. One category of works includes parallel graph processing engines (e.g., Pregel [20] or PBGL [11]) and various improvements

for algorithms and implementations such as direction-inversion [12, 27]). The well-known direction-optimization [3] and other work-avoidance schemes are orthogonal to our work and can be implemented on top of SlimSell; see Figure 1. In general, we do not focus on improving the well-studied queue-based BFS algorithm, but instead apply changes to the graph representation to improve performance.

There are several works on vectorization and GPUs for BFS [25, 22, 6, 29, 9, 12]. Yet, they use queue-based approaches or sparse matrix-sparse vector products and thus suffer from the common downsides such as bad data locality, irregular data accesses, and SIMD or vectorization underutilisation [6]. Contrarily, we start from sparse-matrix dense-vector products as a basis for SlimSell that come with regular memory accesses and better SIMD utilization. The SlimSell optimization for unweighted graphs is applicable not only to Sell- C - σ but also other sparse matrix formats such as ELLPACK/ELL, sliced ELLPACK [23], ESB [17], ACSR [2], and CSR. They all address general matrices and thus use the *val* array with matrix values that can be omitted to reduce data transfer. Next, SlimSell removes padding and thus storage overheads inherent in ELLPACK, differs from ELLPACK/ELL and ESB as it turns the graph storage layout by 90 degrees in memory along with Sell- C - σ to utilize more of SIMD compute power, and targets not only GPUs (like sliced ELLPACK or ACSR) or only KNL (like ESB), but can be used for both and for CPUs. Finally, our work is the first to conduct a systematic analysis on using different semirings for BFS and on work complexity of BFS for miscellaneous graph classes and schemes.

SlimChunk is similar to ACSR [2] and to CSR-VectorL in CSR-Adaptive [8]. Unlike them, we do not adaptively split chunks and instead let the dynamic nature of the partial chunk allocation deal with work imbalance. The advantage of our approach lies in its simplicity: no complex adaptive schemes are required. In addition, SlimChunk is by default enabled only for GPUs as this is the only architecture that entailed load imbalance. Thus, SlimSell offers an intuitive

and simple design for CPUs and Xeon Phi. Another similar scheme is SELL-P [1]: it pads the rows with zeros to make the row length of each block a multiple of the number of threads assigned to a row. Yet, this is discussed only for GPU-based Krylov solvers. Furthermore, Yang et al. [31] facilitate matrix tiling to enhance temporal locality, a scheme different from SlimSell that uses Sell- C - σ to turn the matrix layout by 90 degrees for better SIMD utilization, reduces work and storage overheads to limit the pressure on the memory subsystem. Next, Gunrock [28] is a CUDA library for graph-processing on GPUs. It does not prescribe a high-performance graph representation, but instead provides a high-level, bulk-synchronous, data-centric abstraction that allows programmers to quickly develop new graph primitives. SlimSell could substitute graph representations used by default in Gunrock for higher speedups; an idea that we leave for future work. Another thread of future work is to port SlimSell to massively threaded systems such as SPARC64 or Adapteva Parallel.

Some work has been done into the formulation and implementation of BFS based on the algebraic formulation. Examples include GraphBLAS [21], Combinatorial BLAS (CombBLAS) [4], and BFS with 2D adjacency data distribution [5]. SlimSell, SlimWork, and SlimChunk can be used to accelerate CombBLAS. Finally, our first systematic discussion and theoretical analysis of BFS based on various semirings may be incorporated into the theoretical GraphBLAS framework.

VI. CONCLUSION

Vectorization and throughput-oriented GPUs are reshaping graph processing: traditional BFS codes optimized for latency-oriented CPUs will be inefficient on systems with wide SIMD units. We address this trend and propose SlimSell: a vectorizable graph representation for BFS based on sparse matrix-dense vector products. SlimSell augments the state-of-the-art Sell- C - σ matrix storage format along three dimensions: size, work, and load balance. It effectively applies the regular SIMD parallelism to irregular graph traversals to match or outperform in various scenarios optimized Graph500 codes tuned for high-performance CPUs.

Furthermore, our work provides the first systematic analysis of the formulation, performance, and work/storage complexity of algebraic BFS variants based on different semirings. We derive bounds for uniform and power-law graphs; our theoretical insights combined with performance studies for state-of-the-art architectures such as Intel Knights Landing can be used by architects and developers to improve heuristics and graph representations implemented in processing engines such as CombBLAS [4].

Finally, we strongly believe that SlimSell can be used to accelerate other graph algorithms. Potential speedups can be much higher because BFS is a data-driven scheme with different memory access patterns across iterations while many algorithms (e.g., Pagerank) have identical communication patterns in each superstep.

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