Access

We currently have a server with two Xeon Phi cards. The machine is called **einstein.inf.ethz.ch**. Get in contact with Timo Schneider if you want to have access to it.

Usage

To run a program on the MIC in native mode, write the program in the same way as you would for a multicore Xeon CPU, using OpenMP pragmas, and write your code so that it can be vectorized (Xeon Phi supports 512 bit vector instructions).

Below we show an example program, stored in a file named `test.c`:

```
#include <omp.h>
#include <stdio.h>

int main(int argc, char** argv) {

        int nthreads, tid;

        #pragma omp parallel private(nthreads, tid)
        {
                tid = omp_get_thread_num();
                nthreads = omp_get_num_threads();
                printf("Hello from thread %i of %i\n", tid, nthreads);
        }

}
```

Compiling this can be done with

```
$ icc -mmic -fopenmp test.c -o test.mic
```

I recommend the suffix `.mic` for executables build for the Xeon Phi, but of course you can name your files however you want.

Now create a batch script, similar to this one, which can be named `test.sh`:

```
#!/bin/sh
#SBATCH --gres=mic:1 -n 1 -N 1
export SINK_LD_LIBRARY_PATH=/opt/intel/composer_xe_2015/lib/mic/
srun --gres=mic:1 micnativeloadex ./test.mic
```

The SINK_LD_LIBRARY_PATH specifies the paths where dynamic libraries needed to run the program will be searched. In our case we need this line so that the Intel OpenMP library can be found (libiomp5.so).

Now batch your job via

```
$ sbatch ./test.sh       <-- Command used to start your job
Submitted batch job 29   <-- Output which tells you your job id
$ head slurm-29.out        <-- let's look at the output
Hello from thread 0 of 240
Hello from thread 12 of 240
...
```

See Also

Some links about Xeon Phi:

1. http://vr-zone.com/articles/xeon-phi-knights-series-continues-landing-2015/64112.html [http://vr-zone.com/articles/xeon-phi-knights-series-continues-landing-2015/64112.html]
2. http://www.extremetech.com/extreme/171678-intel-unveils-72-core-x86-knights-landing-cpu-for-exascale-supercomputing [http://www.extremetech.com/extreme/171678-intel-unveils-72-core-x86-knights-landing-cpu-for-exascale-supercomputing]